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Power Dissipation of WSe_2 Field-Effect Transistors Probed by Low-Frequency Raman Thermometry

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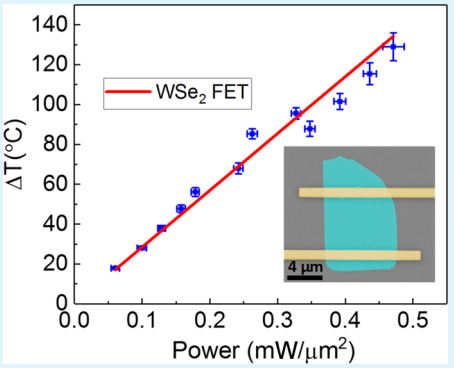
Supporting Information

ABSTRACT: The ongoing shrinkage in the size of two-dimensional (2D) electronic circuitry results in high power densities during device operation, which could cause a significant temperature rise within 2D channels. One challenge in Raman thermometry of 2D materials is that the commonly used high-frequency modes do not precisely represent the temperature rise in some 2D materials because of peak broadening and intensity weakening at elevated temperatures. In this work, we show that a low-frequency E^2_{2g} shear mode can be used to accurately extract temperature and measure thermal boundary conductance (TBC) in back-gated tungsten diselenide (WSe_2) field-effect transistors, whereas the high-frequency peaks (E^1_{2g} and A_{1g}) fail to provide reliable thermal information. Our calculations indicate that the broadening of high-frequency Raman-active modes is primarily driven by anharmonic decay into pairs of longitudinal acoustic phonons, resulting in a weak coupling with out-of-plane flexural acoustic phonons that are responsible for the heat transfer to the substrate. We found that the TBC at the interface of WSe_2 and Si/SiO_2 substrate is ~16 MW/m^2 K, depends on the number of WSe_2 layers, and peaks for 3−4 layer stacks. Furthermore, the TBC to the substrate is the highest from the layers closest to it, with each additional layer adding thermal resistance. We conclude that the location where heat dissipated in a multilayer stack is as important to device reliability as the total TBC.



KEYWORDS: *WSe_2, power dissipation, Raman thermometry, thermal boundary conductance, 2D materials, thermal transport, Boltzmann transport*

INTRODUCTION

The demand for further miniaturization of nanoelectronics[1−7] with high-density vertical integration provides an excellent opportunity for two-dimensional (2D) materials to rival conventional silicon technology.[8,9] Successful implementation of these thin materials within the architecture of future devices could enable the fabrication of field-effect transistors (FETs) with sub-nanometer channel thickness and minimized short-channel effects.[10−13] However, weak energy transport through the van der Waals (vdW) interface of 2D materials with their three-dimensional (3D) underlying substrates could impose a serious challenge for the practical application of these materials because of thermal management issues.[14−16] To shed light on this problem, we performed Raman thermometry experiments and first-principles calculations to characterize the thermal boundary conductance (TBC) at the interface of tungsten diselenide (WSe_2) and a Si/SiO_2 substrate, within an FET platform, at different applied powers. WSe_2 is selected because of its semiconducting behavior with a high charge carrier mobility (e.g., extrinsic back-gate electron mobility of 142 cm^2 V^{-1} s^{-1} for the monolayer).[17,18] However, its low in-plane thermal conductivity (3.935 W m^{-1} K^{-1} for 1 μm WSe_2 sample size[19]), coupled with the small cross-sectional area, makes the role of TBC more critical for heat dissipation during device operation. Furthermore, the lowest thermal conductivity of any solid was measured in the cross-plane direction of disordered WSe_2.[20] In this study, we employed a low-frequency shear-mode peak of WSe_2 Raman spectra to measure the TBC of back-gated WSe_2 transistors.

RESULTS AND DISCUSSION

WSe_2 flakes were exfoliated from bulk powder (Alfa Aesar Company) by standard mechanical exfoliation onto the silicon substrate with a 300 nm oxide layer. Source−drain metal electrodes were patterned by e-beam lithography, followed by the deposition of 5 nm silver (Ag) and 35 nm gold (Au). The inset in Figure 1a shows the colored scanning electron microscopy (SEM) image of a typical fabricated device with

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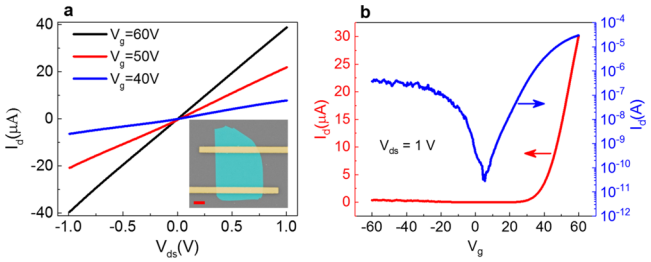

Figure 1. (a) Electrical transport characteristic of WSe_2 FET. The inset shows the colorized SEM image of the back-gated WSe_2 FET (scale bar is 2 μm). (b) Electrical transfer characteristic of WSe_2 FET in the vacuum environment.

a length and a width of ∼6.5 and ∼8.5 μm, respectively. The I_d−V_{ds} measurements in the vacuum environment at three different applied gate biases (Figure 1a) show linear behavior, implying an ohmic contact between Ag electrodes and WSe_2, which is consistent with a previous study.[18]

Figure 1b shows the electrical transfer characteristics (I_d−V_g) of the device measured by applying 1 V source−drain bias and sweeping the gate voltage from −60 to +60 V in vacuum. The measurements indicate an ambipolar behavior with an extrinsic back-gate electron mobility of ∼65 $cm^2\ V^{-1}\ s^{-1}$ and a small hole current at high negative gate voltages (2 orders of magnitude lower than that of the electrons).[18] We have also investigated the effect of current annealing on the mobility of our devices by applying a large (e.g., 10 V) drain−source bias. After this process, the mobility of some of the devices has improved by up to a factor of 2 (Figure S1). The range of back-gated extrinsic electron mobility values for six different fabricated devices varies from ∼20 to ∼70 $cm^2\ V^{-1}\ s^{-1}$ with I_{ON}/I_{OFF} ratio of higher than 10^6. Figure S2 shows the atomic force microscopy (AFM) image of the WSe_2 flake for the device shown in Figure 1a. The height profile shows a thickness of ∼7 nm for this flake.

Because Raman thermometry measurements are taken in the air environment, we tested the I_d−V_g experiments of WSe_2 FET under ambient conditions. However, the results (Figure S3, black) show that the measured current reduces by about 2 orders of magnitude when the device is exposed to air. This could be due to the absorption of moisture from the air, which increases the induced charge traps.[21,22] To passivate the WSe_2 channel, we deposited a 20 nm AlO_x layer directly on top of the flakes using atomic layer deposition (ALD). Figure S4 shows AFM images of the AlO_x layer deposited at 150 and 200 °C on top of the WSe_2 flakes. The height profiles from the surface of these flakes show nonuniform deposition of the AlO_x layer with many pinholes, which caused degradation in the device performance under the ambient condition. Increasing the temperature of the growth from 150 to 200 °C did not improve the quality of the deposition layer but resulted in island-by-island deposition of this layer on top of the WSe_2 flake. We found that the deposition of 1 nm SiO_x layer as a seeding layer by e-beam evaporation followed by the deposition of 20 nm AlO_x layer in the ALD system at 150

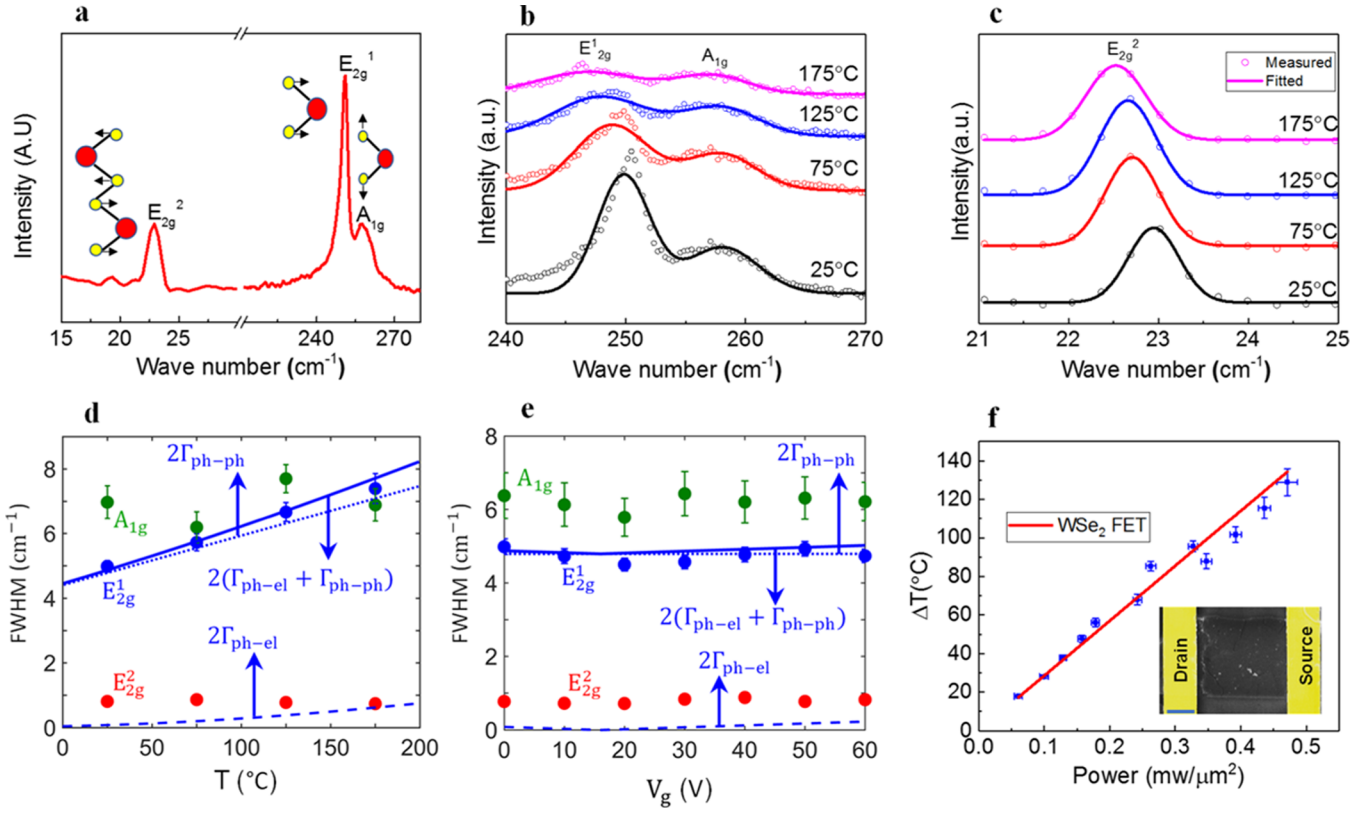

Figure 2. (a) Raman point spectra from the WSe_2 flake. (b) E^1_{2g} and A_{1g} Raman peaks of WSe_2 at different temperatures. (c) E^2_{2g} Raman peak of WSe_2 at different temperatures. (d) Measured (symbols) and calculated (lines) fwhm vs temperature at zero gate voltage. (e) Experimentally measured fwhm vs gate voltage for A_{1g}, E^1_{2g}, and E^2_{2g} modes at room temperature (symbols) and calculated fwhm due to phonon−electron and phonon−phonon interactions (lines). (f) Temperature rise vs applied powers for the channel of the WSe_2 FET. The inset shows the false-colored SEM micrograph of the device after the breakdown test (scale bar is 1 μm).

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°C is needed to form a uniform layer of AlO_x. The AFM image (Figure S5) from the surface of the WSe_2 flake after the passivation of the AlO_x layer by this method shows an average roughness of ∼1.5 nm. To establish electrical connections to the device, the AlO_x layer was etched away from the gold pad areas by using a chlorine etch system (see the Methods section for more details).

Transfer characteristic measurements were performed under the ambient condition to test the stability and performance of devices. Results of the I_d-V_g measurement are shown in Figure S3 (green) at V_{ds} = 1 V. We did not observe a noticeable change in the mobility of the passivated device measured under ambient conditions compared with the non-passivated device tested in a vacuum environment (Figure 1b). However, the maximum current of the device at V_g = 60 V was decreased by a factor of ∼2 compared to the maximum current seen in the vacuum environment, but the device operation remained steady for the entire duration of the subsequent tests. We note that the AlO_x passivation results in 14-fold improvement in mobility compared with the bare devices in air.

Next, confocal Raman spectroscopy at low laser powers (<7.5 $\mu W\ \mu m^{-2}$, laser spot diameter ≈ 1.3 μm) was utilized to obtain the Raman spectra of the WSe_2 flakes under the thermal equilibrium condition. Figure 2a exhibits the characteristic Raman peaks of the WSe_2 flake acquired from the fabricated WSe_2 FET. The E^1_{2g}, A_{1g}, and E^2_{2g} peaks correspond to the in-plane, out-of-plane, and interlayer vibration of atoms, respectively.[23] It is worth noting that Horiba's ULF Bragg filter was used to detect the E^2_{2g} low-frequency Raman peak. For Raman thermometry measurements, the Raman peak shift of WSe_2 FET was first calibrated versus temperature. Figure 2b,c shows the temperature dependence of E^1_{2g}, A_{1g}, and E^2_{2g} Raman-active peaks, respectively. We fitted each individual Raman peak with a Gaussian curve to obtain the full width at half-maximum (fwhm). The extracted fwhm values of E^1_{2g}, A_{1g}, and E^2_{2g} peaks at several temperatures are shown by blue, green, and red markers, respectively, in Figure 2d. The two high-frequency Raman-active peaks, E^1_{2g} and A_{1g}, show large fwhm compared to the E^2_{2g} peak at all temperatures. The broadening of E^1_{2g} increases significantly with temperature and, when coupled with reduced intensities at high temperatures, could result in substantial errors in the thermometry measurements. We explain this trend by simulating all of the possible anharmonic decay channels of the Raman-active high-frequency modes. We calculate the phonon dispersion using density functional perturbation theory (DFPT), described in the Methods section and elaborated in section S6, and find the energy of the Raman-active mode to be $\hbar\omega_{op}$ = 30 meV, based on Figure S6a. The decay of a high-frequency Raman-active mode into a pair of lower frequency modes requires simultaneous conservation of energy and momentum,[24] as discussed in detail in section S7. Our simulations show that of all the possible decay paths shown in Figure S7a, the simultaneous energy and momentum conservation conditions strongly favor the decay into two longitudinal acoustic (LA) phonons, each having one-half the energy $\hbar\omega_{LA} = \hbar\omega_{op}/2$ = 15 meV, as the most frequent decay channel, shown in the inset of Figure S7a. The OP → LA + LA decay is typically called the Klemens channel[25] (see the schematic in Figure S7b), and it leads to a fwhm proportional to $\Gamma_0[2N_0(\omega_{LA},T) + 1]$, where N_0 is the Bose−Einstein distribution function. The resulting temperature trend of fwhm due to the anharmonic phonon−phonon interaction ($fwhm_{ph-ph} = 2\Gamma_{ph-ph}$), driven by N_0, is shown by the blue dotted line in Figure 2d. A Γ_0 = 0.68 fits our experimental data for E^1_{2g} quite well. The blue solid line in Figure 2d represents the total line width obtained by summing the contribution from phonon−phonon ($2\Gamma_{ph-ph}$ shown by the dotted blue line) and phonon−electron interactions ($2\Gamma_{ph-el}$ shown by the dashed blue line). In contrast, because of symmetry rules, A_{1g} modes decay into one optical and one acoustic phonon, which is popularly known as the Ridley decay channel.[25,26] However, there exists a strong interaction between out-of-plane modes and the substrate,[27] which is further enhanced by encapsulation.[16] As a result, the width of the A_{1g} peak displays a weaker temperature dependence (see section S7 for further details).

The coupling between the low-frequency out-of-plane flexural acoustic (ZA) phonons, which are the main carrier of heat into the substrate, and high-frequency optical phonon modes is weak because their interaction is largely prohibited by reflection symmetry,[28] which requires an even number of flexural modes to interact. This leads to strong nonequilibrium among all phonon branches, which renders the extraction of lattice temperature from the shift in Raman frequency of optical modes, E^1_{2g} and A_{1g}, unreliable.[29] On the other hand, the low-frequency E^2_{2g} mode shows a sharp peak (smaller fwhm) even at high temperatures, as shown in Figure 2c. Thus, in this study, we used the frequency shift of the E^2_{2g} mode for Raman thermometry to extract TBC values. Moreover, we found that the line widths of the E^1_{2g}, A_{1g}, and E^2_{2g} modes exhibit only a weak dependence on gate voltage (Figure 2e), suggesting that phonon−phonon interactions are the dominant contributor to Raman line widths.[30] We derive expressions for the line widths due to phonon−electron coupling and plot the resulting contribution to fwhm ($=2\Gamma_{ph-el}$) as dashed blue lines in Figure 2d,e, showing that this contribution is relatively small for the Raman-active modes. The electron−phonon coupling rates are calculated and further discussed in the Supporting Information (section S8). The temperature dependence of $fwhm_{ph-el}$ for different gate voltages is shown in Figure S8a,b. Besides broadening, we also observe that the difference between the frequencies of A_{1g} and E^1_{2g} peaks increases with temperature. Similar shifts in frequencies for Raman-active modes have been observed in few-layer MoS_2,[26] where the E^1_{2g} mode exhibits a stronger shift than that of A_{1g}; it has been attributed to the temperature contribution from thermal expansion and phonon anharmonicity. Previous studies[31,32] report this difference in frequencies to be also dependent on the number of layers (NL), and this thickness-dependent $\omega_{A_{1g}} - \omega_{E^1_{2g}}$ has been attributed to the interlayer coupling in TMDs.

To measure the temperature rise of the WSe_2 channel and silicon substrate under device operation, the Raman peak shifts were first calibrated based on the applied gate voltage of 60 V (Figure S9). The temperature rise was then calculated from the acquired Raman spectra at different applied powers (at 60 V gate voltage) and calibration curves (Figure S10a,b). Figures 2f and S11 exhibit the temperature rise versus applied powers for the WSe_2 channel (based on the E^2_{2g}) and silicon, respectively. For instance, the temperature rises of ∼110 and 10 °C were found for the WSe_2 channel and silicon substrate, respectively, at an applied power density of 0.4 $mW/\mu m^2$.

To determine the TBC between the WSe_2 channel and the substrate, we considered an equivalent thermal circuit from the WSe_2 flake to the silicon substrate (Figure S12). All of the

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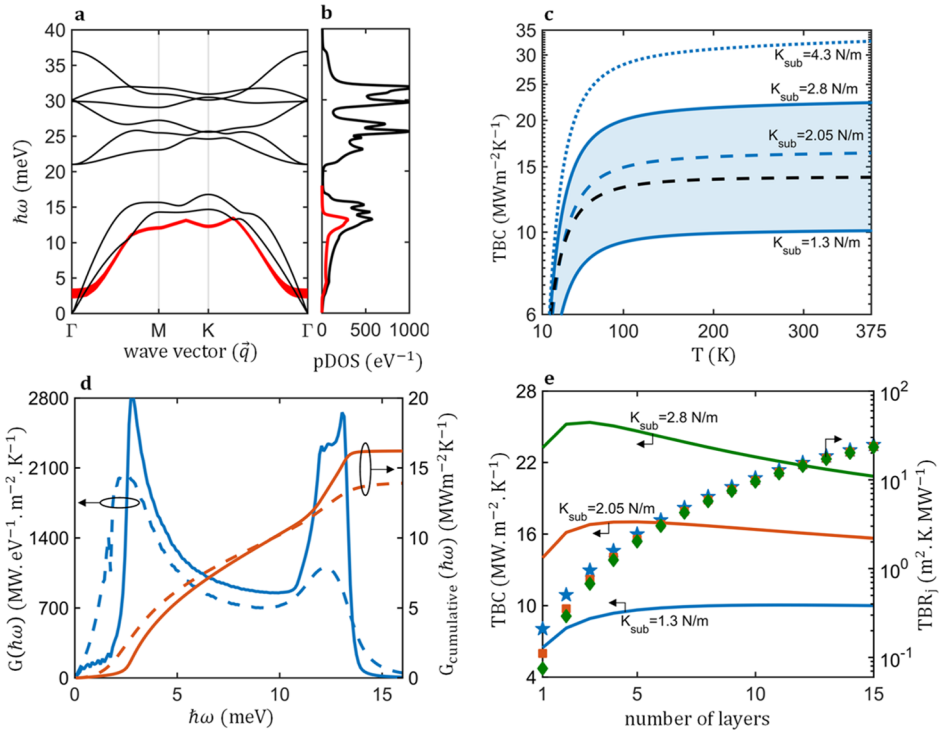

Figure 3. (a) Full phonon dispersion of an 11-layer WSe_2 with 11 gapped flexural modes highlighted in red. (b) Calculated pDOS of WSe_2 (black line), where the pDOS of the gapped flexural branches is highlighted in red. (c) TBC as a function of temperature from 10 to 375 K for encapsulated WSe_2 on SiO_2. The blue lines represent values for an 11-layer stack, whereas the dashed black line represents a single layer with K_{sub} = 2.05 N m^{-1}. (d) Spectral TBC (blue) and cumulative TBC (red) as functions of phonon energy $\hbar\omega$. (e) TBC (left axis only) as a function of the NL (solid lines) in the WSe_2 few-layer stack and the TBR contribution per layer (right axis only) in a 15-layer stack (symbols). Colors of the symbols correspond to the colors of the solid lines for values of K_{sub}.

fabricated devices for Raman thermometry measurements had the length of >4 μm; thus, the in-plane heat conduction can be neglected because of large device dimensions compared with the lateral thermal healing length of the device.[11,33,34] As a result, the total thermal resistance between the hot and cold zones can be considered as a sum of the thermal resistance between the WSe_2 flake and the SiO_2 substrate (R_{int}), the thermal resistance of SiO_2 (R_{SiO_2}), and the thermal resistance of silicon (R_{Si}). The resistance between Si and SiO_2 is neglected because of their low thermal boundary resistance (TBR) (R_{oxs} = 10^{-8} m^2 K/W near room temperature).[34−36] The total thermal resistance of the device ($R_{th} = \Delta T/P$) was extracted from the slope of Figure 2f. Also, the thermal resistance of the silicon substrate can be calculated based on either the slope of Figure S11 or the known values for the thermal conductivity of silicon.[34] We found that TBC values for six tested devices with the same thicknesses (~7 nm) vary in the range of 10−32 MW/m^2 K (Table S1, section S13) using TBC = $1/(A{\cdot}R_{int})$, where A is the area of the device and R_{int} is the thermal resistance between the WSe_2 channel and the SiO_2/Si substrate. Moreover, we investigated the electrical breakdown characteristic of WSe_2 devices. Figure S13 shows a typical I_d−V_{ds} result before and after the breakdown test. The maximum current of 49 μA/μm was recorded at V_{ds} = 80 V right before the breakdown point. This provides a power density of 1.184 mW/μm^2 for most of the tested devices, implying an average temperature of ~370 °C for the WSe_2 channel at the breakdown point. The SEM (inset of Figure 2f) and AFM (inset of Figure S13) images of the WSe_2 FET after the breakdown test reveal that the failure happened near the drain electrode.

To model the transfer of phonons from the encapsulated few-layer WSe_2 stack to its underlying SiO_2 substrate, we used a combination of density functional theory (DFT) and phonon Boltzmann transport equation. We first calculated the full phonon dispersion of monolayer (1H phase) WSe_2 from first principles. We then modified the dispersion of the flexural ZA branch to include gapping because of the coupling to the substrate and branching due to interlayer coupling, as described in the Methods section. In vdW monolayers, the ZA phonon branch is the main contributor to thermal heat transfer into the substrate.[27] In multilayers, each of the N layers in the vdW stack contributes one distinct ZA branch and thus adds to the total TBC. We modified our previously developed 1-layer 2D−3D TBC[16] for N-layer vdW stacks, following the formulation by Ong on multilayer TBR.[37] The multilayer TBC model, including the effect of encapsulation by the AlO_x layer, is further described in the Supporting Information (section S15).

Taking the N-layer WSe_2 film to be ~7 nm thick (based on AFM measurements in Figure S2) and the combined thickness of the trilayer (Se−W−Se) and the vdW gap to be 6.45 Å,[38] we estimated the NL to be 11. Figure 3a shows the phonon dispersion of an 11-layer WSe_2 stack, where we can see the collection of 11 flexural modes highlighted in red. Similarly, Figure 3b shows the phonon density of states (pDOS) of the 11-layer WSe_2, where the pDOS of the ZA branches is highlighted in red. Figure 3c shows the calculated TBC as a function of temperature for an encapsulated 11-layer WSe_2 stack on SiO_2 for various values of vdW coupling constants

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K_{sub}. The blue shaded region spans a range of K_{sub} = [1.3, 2.8] N/m with a median value of 2.05 N/m (blue dashed line) corresponding to TBC values of [10, 22] MW/m^2 K and 16.15 MW/m^2 K, respectively. Increasing the coupling to K_{sub} = 4.3 N/m recovers the highest measured value of 32 MW/m^2 K. The black dashed line corresponds to the TBC of a 1-layer WSe_2 on SiO_2, where we see a smaller TBC as a result of only one layer contributing to the overall TBC, whereas each of the layers in the 11-layer sample contributes to the total TBC.

Figure 3d shows the room-temperature spectral TBC (blue line) and the cumulative TBC (red line) as functions of phonon energy. The solid lines refer to an 11-layer stack, whereas the dashed lines represent a 1-layer stack. In both cases, we see two distinct peaks in the spectral TBC, a larger one in the range 2.5−3 meV (22−25 cm^{-1}), just above the gap caused by the substrate interaction and overlapping with the E^2_{2g} Raman mode, and a smaller peak at around 13 meV from the zone-edge van Hove singularity of the ZA branch. In moving from 1 to 11 layers, the spectral TBC sees an upward shift in energy and increased height of the first peak because of interlayer coupling and additional ZA branches in the dispersion. As a result, we see an increase in the total TBC from 1 to 11 layers. To further probe the thickness dependence of the TBC of the encapsulated few-layer WSe_2 on SiO_2, in Figure 3e we plot the TBC (left axis) as a function of NL in the vdW stack for several values of substrate coupling constants. For weak substrate coupling and small values of K_{sub} (i.e., K_{sub} = 1.3 N/m), the TBC increases monotonically with the number of the layers, the same trend as previously calculated for bare (unencapsulated) few-layer graphene[37] and measured in few-layer MoS_2, both on SiO_2.[39]

In contrast, as K_{sub} increases in the encapsulated multilayer WSe_2, we observe a peak in the thickness dependence of TBC in Figure 3e. For K_{sub} = 2.05 and 2.8 N/m, the TBC peaks at 4 layers and 3 layers, respectively, and then slowly declines with additional layers. This trend is different from the previous work and caused by encapsulation, which improves TBC in monolayers[40] by increasing damping and enhancing the transmission of low-frequency flexural phonons to the substrate. In a multilayer, the layer closest to the substrate contributes most to the TBC but benefits less from encapsulation when there are many layers added on top of it. To elucidate this point, we plot individual contributions from each layer in a 15-layer WSe_2 on the right-hand side y-axis of Figure 3e. The per-layer TBR ($TBR_j = TBC_j^{-1}$) is indicated by symbols (star, square, and diamond), whereas the x-axis stands for the jth layer in a 15-layer stack. The color of the symbols corresponds to the colors of the lines for the three values of K_{sub}. Most of the TBC comes from the first three layers closest to the substrate where the TBR is the lowest (TBR_{1-3} < 1 m^2 K/MW, depending on K_{sub}), whereas the TBR increases steadily for layers away from the substrate, indicating an additional interlayer TBR. After 8 of the 15 layers, the TBR_j of each layer converges to the same value because the resistance between consecutive layers is dominated by the interlayer coupling K_z rather than K_{sub}. Hence, stronger substrate adhesion favors few-layer WSe_2 because most of the heat transfer is contributed by the first few layers closest to the substrate, whereas in the case of weak substrate coupling, a multilayer stack or bulk WSe_2 would result in largest total TBC. In all cases, the location where heat is dissipated in the vertical stack will impact its removal via substrate. Because of the large Thomas−Fermi screening length ($\lambda_{TF} \approx 7$ nm) and interlayer resistance in TMDs, the location of Joule heating in the multilayer stack varies with the gate voltage.[41] The thickness of our WSe_2 flakes is 7 nm, comparable to λ_{TF}, so we do not expect large variations of dissipation in the vertical direction in our measurements. The impact on heat removal would be more pronounced in samples thicker than λ_{TF} and at larger carrier concentrations.

CONCLUSIONS

In summary, we investigated the power dissipation of WSe_2 FETs under electrical operation using the low-frequency Raman mode. We found that the typical E^1_{2g} and A_{1g} peaks do not provide accurate temperature information because of peak broadening and intensity weakening at elevated temperatures. Our experimental and DFT results revealed that the low-frequency E^2_{2g} shear mode, which overlaps with the ZA modes, can be used to measure the temperature rise of the WSe_2 channel and determine TBC values. We also showed that the TBC at the interface of WSe_2 and Si/SiO_2 varies with the number of layers. The conductance is highest from the layers closest to the substrate, whereas those away from it suffer from additional interlayer resistance. We conclude that the location where heat is dissipated matters as much as the overall TBC.

METHODS

AlO_x Deposition. The Savannah-ALD system was used for this process. The WSe_2 samples were transferred to the ALD chamber directly after exfoliation and annealing at 200 °C in the presence of the argon gas. The system pumped down immediately to remove the unwanted gases from the deposition chamber. Then, 20 nm Al_2O_3 layer was deposited on top of the flakes by using water as an oxygen source and trimethylaluminum (TMA) as an aluminum source. During the process, TMA was purged into the chamber by a pulse time of 0.015 s, and after 8 s waiting time, the water was also purged into the chamber by a pulse time of 0.018 s. During the process, 5 standard cubic centimeters per minute (sccm) nitrogen gas was purged into the chamber as a carrier and venting gas.

AlO_x Etch Process. To establish an electrical connection to devices after the deposition of the Al_2O_3 layer, we etched the layer from the gold-pad areas. The Plasma-Therm ICP chlorine etch system was used for this process. Boron trichloride (BCl_3; 5 sccm) gas was used to etch the Al_2O_3 layer, and the power of the system was set at 100 W. Argon gas (15 sccm) was also flown during the entire process, and it took about 6 min to etch the 20 nm Al_2O_3 layer.

Calculation of Phonon Dispersion and TBC. We calculated the full phonon dispersion from DFPT as implemented within the Quantum ESPRESSO[42] package. The dispersion of the flexural branches that contribute to the TBC in the N-layer stack is gapped by coupling to the substrate and split into N subbranches by interlayer coupling. The modification of the flexural ZA phonon branch dispersion due to these interactions can be written as $\tilde{\omega}_{j,ZA}(\vec{q}) = \sqrt{{\omega_{ZA}}^2(\vec{q}) + {\omega_0}^2 + \frac{2K_z}{M_{WSe_2}} \sin^2\left[\frac{(j-1)\pi}{2NL}\right]}$, where $\omega_{ZA}(\vec{q})$ is the as-calculated DFPT phonon dispersion of the ZA branch of WSe_2, ω_0 is the gapping of the first monolayer in the stack $\omega_0 = \sqrt{K_{sub}/M_{Se}}$, K_{sub} is the vdW spring coupling constant between the bottommost WSe_2 layer and the substrate, K_z is the interlayer spring coupling constant between adjacent layers of WSe_2[23] taken as K_z = 8.24 N m^{-1}, M_{Se} is the atomic mass of Se, j represents the jth layer in the N-layer vdW stack spanning [1, NL], and NL is the total NL. The dispersion of the gapped ZA branches is next input into our multilayer TBC model to obtain phonon transport from an encapsulated few-layer WSe_2 flake into its underlying SiO_2 substrate. Further details of the phonon dispersion calculation and the multilayer TBC model are described in the Supporting Information (sections S6 and S15,

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respectively). Figure S6 shows the full phonon dispersion and pDOS for the monolayer WSe_2 as calculated from the first principles.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b04724.

Mobility improvement of the devices after current annealing; AFM characterizations of WSe_2 flakes; electrostatic breakdown test; detailed information about first-principles calculation of phonon dispersion of the monolayer WSe_2; derivation of phonon−electron rates; and details about phonon−phonon coupling, optical decay channel, and our multilayer TBC model (PDF)

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Author Contributions

A.S.K. and A.B. conceived the idea. A.S.K. led the fabrication and experiments. Z.A. developed the BTE model and led the first-principles calculations. A.B. developed the fabrication process, experimental setup, and thermal analyses. A.B. and Z.H. fabricated all of the devices. A.B., P.Y., and Z.H. performed Raman thermometry measurements and thermal analysis. C.J.F. performed numerical calculations, and A.K.M. derived phonon interaction rates. All authors contributed to the write-up of the article.

Notes

The authors declare no competing financial interest.

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