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Low-cost, high-performance and efficiency computational photometer design

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ABSTRACT

Researchers at the University of Alaska Anchorage and University of Colorado Boulder have built a low cost high performance and efficiency drop-in-place Computational Photometer (CP) to test in field applications ranging from port security and safety monitoring to environmental compliance monitoring and surveying. The CP integrates off-the-shelf visible spectrum cameras with near to long wavelength infrared detectors and high resolution digital snapshots in a single device. The proof of concept combines three or more detectors into a single multichannel imaging system that can time correlate read-out, capture, and image process all of the channels concurrently with high performance and energy efficiency. The dual-channel continuous read-out is combined with a third high definition digital snapshot capability and has been designed using an FPGA (Field Programmable Gate Array) to capture, decimate, down-convert, re-encode, and transform images from two standard definition CCD (Charge Coupled Device) cameras at 30Hz. The continuous stereo vision can be time correlated to megapixel high definition snapshots. This proof of concept has been fabricated as a four-layer PCB (Printed Circuit Board) suitable for use in education and research for low cost high efficiency field monitoring applications that need multispectral and three dimensional imaging capabilities. Initial testing is in progress and includes field testing in ports, potential test flights in un-manned aerial systems, and future planned missions to image harsh environments in the arctic including volcanic plumes, ice formation, and arctic marine life.

Keywords: photometer, infrared, field programmable gate array, multichannel, stereo vision, depth mapper

1. INTRODUCTION

Computational photography provides processing directly on digital cameras with features such as integration of many snapshots into a single panorama image. In the same way, the CP integrates continuous multi-channel computer vision, digital video and snapshot digital image processing in a single device with features such as depth mapping and generation of mosaic images. The continuous digital video processing for computer vision features is provided by both an FPGA interface and by an embedded Linux microprocessor. Computer vision transform and convolution primitives required by higher level stereo and 3-D computer vision are provided by FPGA state machine logic operating on the input path from the multi-channel analog camera interface to offload the microprocessor to enable it to implement higher level functions such as passive depth mapping. The hardware state-machine also provides deterministic continuous 30Hz transformation. The continuous computer vision functions can also be coordinated with high resolution snapshots at lower non-continuous rates. The FPGA layer performs pixel encoding, time and resolution decimation as well as resolution interpolation required for left and right channel stereopsis. The multi-channel design can likewise be reconfigured for an infrared and visible channel for multi-spectral operation or for active depth mapping with the addition of a structured light infrared projector. The design of the PCB for the multi-channel analog camera interface to the FPGA is intended to be an open hardware reference available for education, computer vision and instrumentation research and product innovation. The ability to use the reference PCB with commonly available FPGA and microprocessor options in small, battery powered systems makes the CP a modular system that can be integrated into a wide variety of computer vision and high definition snapshot collection applications. Several uses that are planned or in consideration will be reviewed in this paper, but first the design concepts, interfaces, and architecture will be provided. The ultimate goal is the make the hardware (the interface PCB between cameras and FPGA boards), reference HDL (Hardware Design Language) firmware (FPGA bit streams), and reference software including OpenCV⁸ applications available for general use to extend and experiment with the design presented here.

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2. COMPUTATIONAL PHOTOMETER DESIGN GOALS

The CP was conceived out of frustration that most analog and digital cameras available for computer vision research and education do not have a balance of affordability, open design, and real-time performance features allowing for quick experimentation with passive 3-D vision algorithms. These algorithms are used in embedded applications to explore biologically inspired processing and to emulate human vision functions¹². Likewise, the CP was designed so students can integrate multi-channel camera systems into educational projects with application specific modifications.

2.1 Off-the-shelf Comparison Methodology

The authors tested many cameras and depth mappers like the PrimeSense systems over years keeping track of performance, cost, how open the hardware, firmware and software are, and how efficient the option is for embedding and powering from a battery. This is somewhat subjective and could include far more parameter like resolution, exact power consumption, and specific brands, but the basic analysis is provided here to simply provide justification for the custom PCB and the overall partial off-the-shelf modular design for the CP. Exciting new options like off-the-shelf active depth mappers using the PrimeSense ASIC (Application Specific Integrated Circuits) from ASUS, Microsoft, and others come with an open application programmer's interface (OpenNI³). Unfortunately active depth mapper hardware is largely proprietary and difficult to modify, extend, or integrate directly on a custom PCB and also difficult to probe to learn about digital and analog signaling. The authors concluded that the most cost effective method of providing an open design with capabilities similar to proprietary analog and digital cameras with pre-processing ASICs is to provide a hybrid FPGA and microprocessor reference design.

A table summarizing features and comparing off-the-shelf options with the CP architecture is summarized in Table 1.

The grades for each category in Table 1 are rated 1 to 3 as follows:

1. Cost – 3 if available for less than \$500, 2 if commonly less than \$1000, 1 if commonly more than \$1000.
2. Openness – 3 if hardware (HW), firmware (FW) and software (SW) are open design file and source code, 2 if only two layers are, and 1 if only one layer. In cases where IP can be licensed a half credit was awarded.
3. Performance – 3 if frame rates are nearly constant at 30Hz or better with microseconds of interrupt latency for real-time (RT), 2 if frame rates are 30Hz or better with latency variation in milliseconds, 3 if variable frame rates less than 30Hz are observed most often.
4. Efficiency – 3 if the configuration can be easily battery powered for hours of embedded operation, 2 if the configuration can be embedded at all, 1 if it must be hosted in a lab or pole attached with grid-tied power.

Table 1. Summary of alternative fully off-the-shelf options compared to the modular Computational Photometer (Resolution of 480i/480p considered sufficient, no preference for HD, *performance for the CP is still in verification)

Configuration	Cost	Openness	Performance	Efficiency	Score
CP	Low (3)	Open HW, FW, SW (3)	*RT (3)	High (3)	12
Digital Camera Port ⁵	Low (3)	Proprietary HW, Open FW, SW (2)	Variable (1)	High (3)	9
Analog Camera with PC Frame Grabber	Low (3)	Proprietary HW, Open FW, SW (2)	RT (3)	Low (1)	9
CameraLink ⁴	High (1)	Proprietary HW, IP FW, Open SW (1.5)	RT (3)	High (3)	8.5
USB Webcam or Active Depth Mapper	Low (3)	Proprietary HW, FW, Open SW (1)	Variable (1)	High (3)	8
Ethernet CCTV ⁶	Medium (2)	Proprietary HW, FW, Open SW (1)	Predictable (2)	Low (1)	6
HD and SD-SDI	High (1)	Proprietary HW, FW, SW (0)	RT (3)	Low (1)	5

The University of Adelaide tested a number of CCTV security cameras, webcam and analog cameras⁶ and the authors have likewise tested frame rates on CameraPort, webcam, and analog cameras with a frame grabber to establish performance. Software and firmware for analog cameras using video decoders available off-the-shelf as well as a VxWorks driver developed by the authors is available for real-time digital video processing and computer vision¹⁰. Low

cost is important for educational use, high performance for interactive, real-time robotics and process automation using computer vision. Efficiency is essential for embedding in field applications and devices. Open hardware, firmware and software are also critical for education and research. Finally, for product innovation, licensed IP options as are often available for some configurations and open application programmer's interfaces may be sufficient to commercial applications, but solutions meeting all of the author's criteria were not found to be available off-the-shelf.

2.2 Modular Multi-channel Interface Board

The custom PCB that has been fabricated, now being verified by the authors, is intended to bridge two or more analog cameras to an FPGA board that in turn uses standard interfaces to a microprocessor. As such, it is an analog front-end, but with the FPGA reference HDL it provides interface-based image transformation offload as shown in Figure 1.

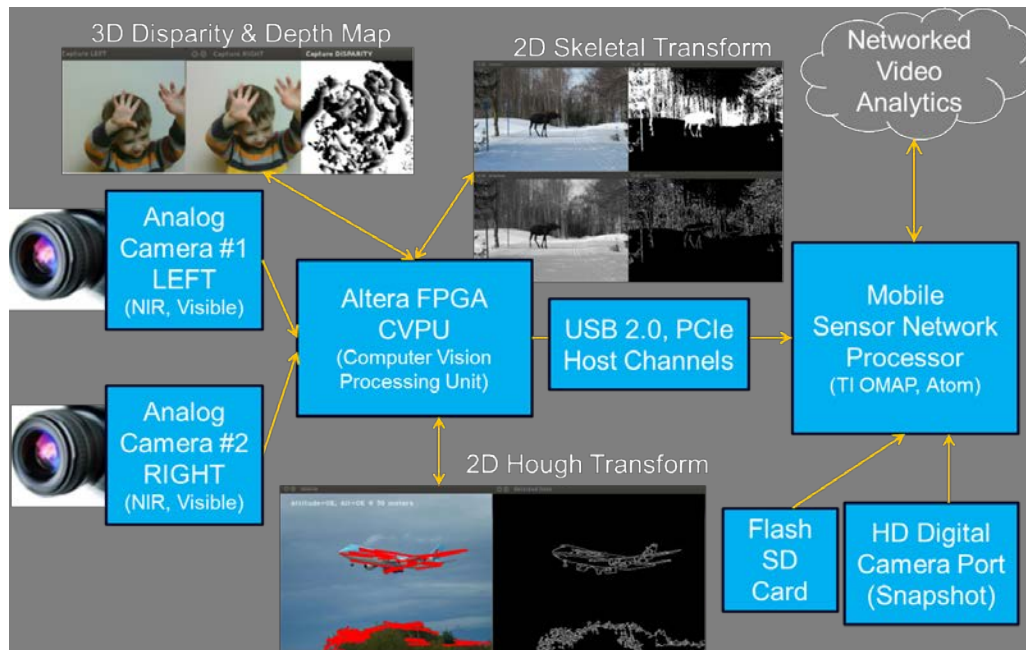


Figure 1. Computational Photometer Block Diagram – Multi-channel Passive Configuration

2.3 Educational Goals

To provide students and faculty a reference design with analog and digital hardware design files that can be easily modified to scale, extend or improve the basic camera to FPGA interface board with simple test interfaces for analog and digital signal probing. The design for the PCB has been kept simple, with a common four layer PCB layout approach to lower cost of fabrication and simplify verification. The design files will ultimately be made available through university program web sites working with our industry sponsors. Exact open hardware and software licensing details have yet to be finalized, but the goal is to follow the lead set by other open hardware reference designs.

2.4 Research Goals

The CP has been designed for a minimum of dual-channel continuous digital video acquisition and coordinated stereo computer vision pre-processing for common keypoint analysis (image registration) methods to compute passive depth maps using stereopsis. Likewise, more sophisticated segmentation, recognition, and point cloud model generation algorithms can be implemented on an interfaced microprocessor like the TI OMAP. The PCB design allows for use with a wide range of Altera DE boards, from the small scale DE0 to the DE2i, providing for simple battery powered use, but also for lab powered or pole attached uses for research with higher bandwidth and multi-core processing.

2.5 Innovation Goals

Potential product innovation and concepts can be explored by leveraging the open hardware, firmware and software design. Our project goal is to encourage and facilitate FPGA acceleration of common computer vision convolutions and transformations found in open source software, e.g. OpenCV, to provide microprocessor offload and to increase

performance and efficiency for applications like active depth mapping. Active depth mappers have potential medical applications such as wound care⁷, intelligent transportation vehicle safety, augmented reality, entertainment and more. Since commercial applications need the option to build proprietary applications, the open license will be formulated to allow for proprietary as long as the core reference design and improvements to it remain open. Initially the reference will simply provide FIFO (First in First Out) buffering of both digital video channels with options to re-encode pixels into several formats from the hardware decoder (YCrCb, RGB, grayscale), resolution decimation and interpolation for down and up conversion, as well as time decimation at the frame level. Longer term, with larger scale FPGA options such as the Altera DE2i, it is envisioned that more complex transforms might be fully offloaded to the FPGA.

Likewise, it is often simpler to interface flash storage, file systems, and to host data management and searching algorithms such as recognition search algorithms built on SIFT, AdaBoost or Haar features² for facial detection and recognition, the generalized Hough¹¹ transform as well as many machine learning and inference applications for computer vision on embedded Linux platforms. The CP design enables this simply by providing a USB 2.0 uplink to low-power microprocessors like the TI-OMAP and on the DE2i, but leveraging the on-board PCI express interface between the FPGA and the multi-core Intel Atom microprocessor. Both can easily be configured to boot Linux, mount file systems, and host a full OpenCV library to simplify and speed-up application development.

The Revision-A PCB was fabricated in January of 2014 and the authors are verifying the functionality of the TI decoders (each channel), the debug and test TI encoder, the parallel-to-I2C firmware configuration interface, and the FPGA digital video output. The major blocks are shown in Figure 2 from the schematic capture tool (Mentor Graphics DxDesigner).

Figure 2. Revision-A Computational Photometer Top Level Schematic

decoding consumes less than a half watt, and FPGA power requirements scale directly with frame rate and computational complexity. Verification completion and release of hardware design files through an open hardware university program is scheduled for late 2014. A picture of the Revision-A PCB is provided in Figure 3.

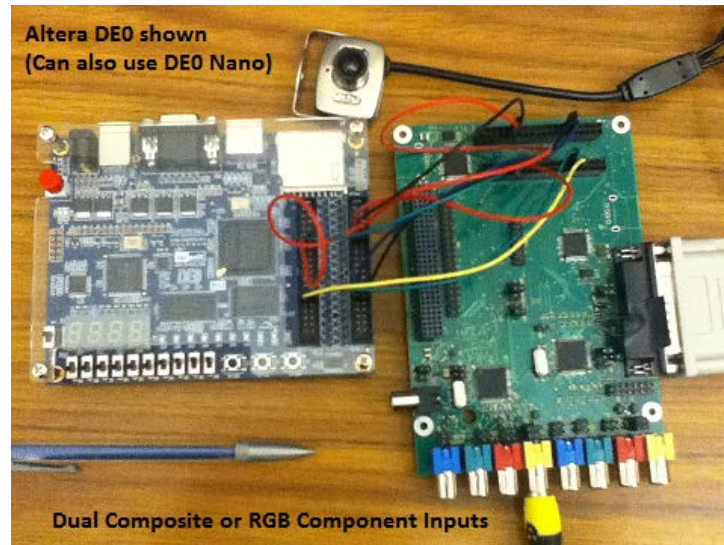


Figure 3. Revision-A Computational Photometer PCB

Note the dual YPrPb (Y=Green luminance gamma corrected with sync, sub-sampled modulated Red, and sub-sampled modulated Green) inputs with alternate composite NTSC input options. The parallel port is a Revision-A feature for debug that can be eliminated, but allows for use of the decoder and encoder firmware configuration tools. Open reference design users can decide to preserve or eliminate debug and test interfaces. Digital video verification is being completed using a second separate FPGA state machine to generate NTSC Y-channel only test input on the component interface to drive in known gray map patterns that can be verified on digital outputs between the decoders and the FPGA. Likewise, injected test patterns can be verified on the UBS 2.0 or PCI express microprocessor interfaces as well.

4. COMPUTATIONAL PHOTOMETER RESEARCH APPLICATIONS

The CP will enable research in both passive 3-D computer vision and active RGB depth mapping⁹ with an infrared or visible structured light projector such as the Texas Instruments DLP (Digital Light Projector) as shown in Figure 4.

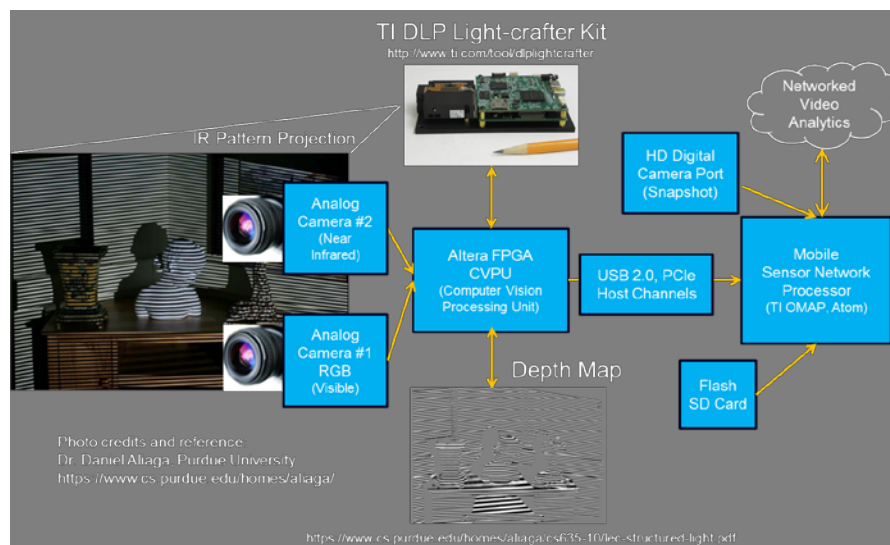


Figure 4. Computational Photometer Active RGB Depth Mapper Configuration

Furthermore, with the use of analog infrared cameras (readily available at reasonable cost, or derived by removing filters), multi-spectral images with correspondence can be used in computer vision research as well. Perhaps most importantly, the CP opens up hybrid FPGA and microprocessor software computer vision algorithm research. The concept of the CVPU is made easier to explore using Altera DE FPGA boards and the CP interface board. For example, the lowest level image convolution and transformation primitives of edge detectors, the steps in SIFT keypoint correspondence for recognition, image stitching, digital stabilization and passive stereopsis can be implemented in the FPGA. Acceleration of SIFT and related feature vector and shape detection (Hough transform) methods are a major goal for research after verification.

5. SUMMARY AND FUTURE PLANS

After verification and release of the CP design described here, future work includes education, innovation and research application work. The performance of FPGA accelerated edge detection convolutions, feature vector matching, shape finding transformations and general resolution interpolation and decimation performance will be reported in future publications by the authors. The hybrid FPGA accelerated applications can be compared to the same applications built with off-the-shelf cameras, software processing only, GPU acceleration, and multi-core processing to quantify the efficiency (in terms of total power used), the frame rate, and the algorithmic metrics such as keypoint matches per second. The authors invite others to help in the overall verification, extension of the design, and would encourage similar testing of computer vision algorithms with FPGA acceleration and sharing of results.

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