Novel three-phase asymmetrical cascaded multilevel voltage source inverter

Saad Mekhilef
Novel three-phase asymmetrical cascaded multilevel voltage source inverter

Hamza Belkamel¹, Saad Mekhilef², Ammar Masaoud¹, Mohsen Abdel Naeim²

¹Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
²Mechanical Engineering Department, Faculty of Engineering, Assiut University, Assiut 71516, Egypt
E-mail: hbelkamel@siswa.um.edu.my

Abstract: Series connection of power cells in asymmetrical cascaded configurations helps to cancel redundant output levels and maximise the number of different levels generated by the inverter. A new configuration of three-phase multilevel asymmetrical cascaded voltage source inverter is presented. This structure consists of series-connected sub-multilevel inverters blocks. The number of utilised switches, insulated gate driver circuits, voltage standing on switches, installation area and cost are considerably reduced. Cascaded-cell DC voltages in each inverter leg form an arithmetic sequence with common difference of E. With the selected inverter DC sources, high-frequency pulse-width modulation (PWM) control methods can be effectively applied without loss of modularity. Low-frequency and sinusoidal PWM techniques were successfully applied. Hence, high flexibility in the modulation of the proposed inverter is demonstrated. The prototype of the suggested inverter was manufactured and the obtained simulation and hardware results ensured the feasibility of the configuration, and the compatibility of both modulation techniques was accurately noted. Lastly, the semiconductor losses in the converter were calculated using simulation models. Based on the analysis of the total power losses, the proposed inverter provided high efficiency at different operating conditions.

1 Introduction

Many multilevel converter topologies and wide variety of control methods have been developed in the recent literatures [1–3]. Three different basic multilevel converter topologies are commonly used, which are the neutral point diode clamped (NPC); flying capacitor (FC) and the cascaded H-bridge (CHB) [4, 5].

The CHB multilevel inverter combines a multiple units of single-phase H-bridge power cells. The prominence of this configuration is attributed to some characteristics lacked in other inverter topologies [6, 7]. This structure needs only standard low-voltage mature technology components to output medium voltage levels. Furthermore, these converters have a high modularity degree, since each inverter can be seen as a module with similar circuit topology, control structure and modulation [8]. Therefore any faulty module in the inverter can be quickly and easily replaced. Moreover, with an appropriated control technique, there is a probability to bypass the faulty module without stopping the load, bringing an almost continuous overall availability [9].

The symmetric structure of CHB inverter makes use of equal DC voltage sources and for N H-bridge cells per phase, there are \(2N+1\) levels produced in output of phase voltage. Each cell of the H-bridge needs a separate DC source, which is usually obtained by an arrangement of three-phase or single-phase diode-based rectifiers [10]. Multiple transformers are used to provide the electrical isolation. Recently, high-frequency transformer-based modules are utilised in building cascaded multilevel inverters [11] without isolated DC links, and diode-based rectifier has been replaced with active front-end rectifier which is more suitable for regenerative operation [12, 13]. In some applications, these DC voltages can be acquired directly by isolating DC sources like photovoltaic panels [14] or DC–DC isolated converters [15].

Asymmetrical cascaded H-bridge (ACHB) inverters use DC supplies with unequal voltages [16]. This topology offers a good opportunity to increase the number of levels with reduced total harmonic distortion (THD) and switching losses. ACHB inverters show high efficiency up to 80% at the fundamental frequency [17, 18].

Furthermore, the number of voltage steps is maximised when the cascaded-cell DC voltages form a ratio-3 geometric sequence [19]. This ratio has been utilised to design inverters with large number of levels and, therefore, small voltage distortion for multifarious applications [20, 21]. However, it has been discovered that ratio-3 DC-sourced inverter is not suitable for high-frequency pulse width modulation (PWM) control techniques as the high-voltage stage is subjected to high switching frequency [22–24].

A two-cell stack that is similar to the generalised topology has been cascaded with three-level FC cell [25]. This configuration significantly minimises the number of the utilised DC supplies, and the size of the capacitors used in high-voltage stage is twice the one of the
low-voltage stage. Such arrangement classifies the topology under the asymmetrical configurations and five voltage levels have been produced. Unfortunately, the proposed structure and the modulation technique may not serve the purpose if more voltage steps are required. Moreover, a large number of switches have been employed and large capacitor banks need to be included in high-voltage applications.

Recently, CHB inverters employ multilevel DC-link and came up with a higher number of total output voltage levels using a single-phase inverters. A variable DC-link voltage provides the single-phase full-bridge (SFPB) inverter with several voltage levels starting from zero volts [26]. Also, the SPFB inverter produces the positive and negative voltages of the supplied voltage. These configurations have the capability to deliver a high output current with low switching frequency in the SPBF. The variable DC-link voltage can be obtained from cascaded NPC or FC structures or even from buck DC–DC converters [27, 28]. The SPBF inverter configuration that consists of a multilevel DC source and a SFPB inverter was presented in [27]. The SPBF inverter is used for creating zero, negative and positive voltages. Unfortunately, the half-bridge-based multilevel DC-link inverter seems too costly because of the symmetric DC supplies and large number of switches used. In [29], the author introduced a novel topology in the family of ACHB with the intent of achieving higher number of voltage levels without increasing the number of switches. An algorithm to determine the DC source levels is provided. Unfortunately, the proposed algorithm does not serve in creating all steps (odd and even) at the output voltage. To produce an output voltage with a constant number of steps, large numbers of bidirectional switches are needed. The aforementioned drawbacks can be overcome based on the proposed work in [26, 30], whereby all even and odd levels can be produced. It was proven that a higher number of steps with a minimised number of switches is used compared to the configuration in [29]. It is noteworthy that both configurations in [26, 30] contributed in lessening of the number of switches and gate driver circuits with minimum standing voltage on the switches, but the topology was not extended to three-phase applications. Moreover, the inverter did not show flexibility in control, since none of the control techniques has been employed. This paper suggests a novel topology for three-phase asymmetrical n-level cascade inverter. Each phase in the proposed topology consists of a series-connected basic units. Based on the desired number of output voltage levels, a number of basic units are used.

The power circuit of the introduced three-phase inverter makes use of unequal DC sources in magnitude. Such characteristic classify it under the asymmetrical multilevel inverter topologies. It is noticeable that the topology

### Table 1

<table>
<thead>
<tr>
<th>State</th>
<th>Switches states</th>
<th>( V_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>2</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

### 2 Proposed topology

Fig. 1a shows the basic unit of the proposed topology. Two switches are used with a single DC supply to output two voltage levels 0 and \( E \). \( S_1 \) and \( S_2 \) are always in inverted conditions. If the switch \( S_1 \) is ON, \( V_o = E \), however, the OFF state of \( S_1 \) makes \( V_o = 0 \). Switches \( S_1 \) and \( S_2 \) cannot be ON simultaneously to avoid the occurrence of short circuit across the DC supply. Table 1 provides the output voltages of the basic unit for different switching states.

Fig. 1b shows the power circuit of the suggested three-phase asymmetrical n-level cascade inverter. Each phase in the proposed topology consists of a series-connected basic units. Based on the desired number of output voltage levels, a number of basic units are used.

The power circuit of the introduced three-phase inverter makes use of unequal DC sources in magnitude. Such characteristic classify it under the asymmetrical multilevel inverter topologies. It is noticeable that the topology
involves numerous DC supplies, especially if a higher number of voltage steps are required. In this case there is the possibility to replace the DC supplies with renewable energy devices such as photovoltaic or fuel cell. The value of DC supply used in each and every basic unit in a particular inverter leg is obtained as follows

\[
V_1 = E \\
V_2 = 2E \\
V_3 = 3E \\
V_n = nE
\]  

(1)

where \( n \) is the number of basic units per inverter leg. The phase to ground voltage \( S \) is the summation of the output voltages of all basic units, as given in (2).

\[
S = V_1 + V_2 + V_3 + \cdots + V_n
\]

(2)

The maximum output voltage is calculated by substituting (1) in (2)

\[
S = E + 2E + 3E + \cdots + nE\]

\[
S = (1 + 2 + 3 + \cdots + n)E
\]

\[
S = E \sum_{i=1}^{n} i
\]

\[
V = \frac{nE}{2}(n + 1)
\]

(3)

The number of steps \( N \) (voltage levels) with respect to the number of the used basic units can be calculated using (4).

\[
N = 2 \sum_{i=1}^{n} i + 1
\]

\[
V = nE(n + 1) + 1
\]

(4)

3 Modulation techniques for the proposed inverter

In multilevel inverter modulation, two groups of methods have been followed according to the switching frequency: modulation with fundamental switching frequency or high switching frequency PWM.

3.1 Low-frequency modulation

The fundamental frequency is considered as a beneficial modulation technique because of its low switching frequency compared to other control methods [27]. The conventional PWM technique, space vector pulse-width modulation (PWM, sub-harmonic PWM (SH-PWM) and switching frequency optimal PWM (SFO-PWM) for multilevel inverters necessitate equal DC voltage sources (symmetrical topologies). For instance, if the fundamental switching scheme is applied using the Elimination Theory, the transcendental equations characterising the harmonic contents (such as the 5th, 7th, 11th and 13th) can be easily transferred to polynomial equations [31].

In order to examine the performance of the proposed inverter, a typical four-level inverter topology is extracted as shown in Fig. 2. The first and the second unit are fed with \( E \) and \( 2E \), respectively. The DC value is taken as \( E = 50 \) V.

The balanced load voltage can be achieved if the inverter operates on the modes depicted in Table 2. The inverter may have 18 different switching states within a cycle of the output waveform.

3.2 Sinusoidal pulse width modulation (SPWM)

The simplest way of producing the PWM signal is through the comparison of a reference sine wave with a triangle wave [32]. As depicted in Fig. 3a, the sine wave and the three carriers (Carrier 1, Carrier 2 and Carrier 3) are compared.

The Boolean outputs of the comparison make the pulsed signals \( C_1, C_2, C_3 \). With some logical operations applied to

![Fig. 2 Proposed three-phase asymmetrical cascade four-level inverter](image-url)
Table 2 Mode of operation of the proposed three-phase multilevel inverter during one cycle

<table>
<thead>
<tr>
<th>Mode</th>
<th>Switching states</th>
<th>Line voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_1</td>
<td>S_2</td>
<td>S_3</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>2</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>3</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>4</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>5</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>7</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>8</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>9</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>10</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>11</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>12</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>13</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>14</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>15</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>16</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>17</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>18</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

C₁, C₂, and C₃ as given in (5) to (8)

\[ G_1 = (C_2 \times C_3) + C_1 \]  
\[ G_2 = (C_1 \times C_2) + C_3 \]  
\[ G_3 = (C_1 + C_2) + C_1 \]  
\[ G_4 = (C_2 + C_3) + C_3 \]  

where \( \times \) stands for logic AND; \( + \) stands for logic OR.

The appropriate switching signals that lead to the desired output waveform can be derived, where \( G_1, G_2, G_3 \) and \( G_4 \) are the gate signals for switches \( S_1, S_2, S_3 \) and \( S_4 \), respectively. To avoid the short-circuit across the DC-link in each and every basic unit, the following statement has to be maintained all the time.

\[ G_1 = \overline{C_2} \text{ and } G_3 = \overline{C_4} \]

In Figs. 3b and c there is an illustration of the gate signals of the four switches in the first leg (phase A) of the suggested multilevel inverter. In order to obtain the gate pulses for the switches in phases B and C, the same process and operations have been followed to control the switches in phase A with a shifted reference signal 120° and 240°, respectively. This feature makes sinusoidal PWM a promising technique especially in three-phase applications.

4 Experimental results and discussions

To ensure the feasibility of the proposed inverter, the power circuit was simulated in MATLAB/Simulink power block set software. The inverter was implemented and its prototype has been manufactured. Insulated-gate bipolar transistors (IGBTs) with anti-parallel diodes (IRG4PH50UDPBF, 24A, 1200V) were employed as switching devices. Digital signal processor (DSP, TMS320F28335) was used to produce the switching signals for the inverter.

Simulation and hardware results have clearly shown the reliability of the low-frequency and SPWM techniques in the control of the suggested inverter. As mentioned earlier, the two basic units in each inverter leg take different voltages, whereas the voltage in the first unit is twice the second unit.

During the hardware implementation, the inverter was tested under \( E = 50 \text{ V} \) in the first unit and \( 2E = 100 \text{ V} \) in the second unit. For SPWM implementation, the modulation index is taken as \( M_i = 0.8 \) with switching frequency \( f_c = 2000 \text{ Hz} \).

The control block diagram of the proposed inverter is depicted in Fig. 4a. The prototype of the proposed inverter that includes the following three high-voltage DC supplies, three low-voltage DC supplies, switching devices, DSP and 20-Ω three-phase resistive load is shown in Fig. 4b.

Figs. 5a and 6a depict the inverter output line to ground voltage using low-frequency and sinusoidal PWM techniques, respectively. Both staircases show four positive voltage levels: 0, \( E \), \( 2E \) and \( 3E \). The presented topology eases the way to come up with the negative voltages (\( -E \), \( -2E \) and \( -3E \)) without any other additional circuits.

It is well known that for \( n \)-level inverter there are \((2n-1)\) line-to-line voltage levels consisting of \((n-1)\) positive levels, \((n-1)\) negative levels and zero (0 V). For four line-to-ground voltage levels in Figs. 5a and 6a, there are seven line-to-line voltage levels, as shown in Figs. 5b and 6b.

In both modulation techniques, the controller manages to generate the appropriate switching signals that lead the inverter to output the desired voltage. The feasibility of the configuration is conspicuous since it offers high flexibility to use different loads with different parameters.

In the topology introduced in [27], five basic cells per phase were utilised to come up with 11 voltage levels. In order to reach such level count in three-phase, 15 equal DC sources categorise the topology under symmetrical inverter. Based on these two characteristics, the inverter requires a considerable number of DC supplies, switches and gate driver circuits as well. In the proposed connection, a multilevel DC-link is used without the H-bridges and the DC supplies are taken asymmetrically as described in Section 2. Figs. 6b and 7a clearly show the substantial...
increment in the inverter output voltage levels with a reduction in power electronics components and DC supplies. Table 3 calculates the needed DC supplies and switching devices to produce 11 line-to-ground voltage levels using the proposed topology in [27] and the configuration suggested in this paper.

The proposed configuration has been tested under different modulation indices. The THD of the output voltage can be calculated by

\[
\text{THD} = \sqrt{\sum_{n=3,5,7,\ldots} V_n^2} / V_1
\]  

(10)

where \( V_1 \) and \( n \) are the fundamental component and harmonic order, respectively. Fig. 8a shows the variation in THD with

---

**Fig. 3** SPWM showing

a) Sinusoidal pulse-width modulation (SPWM)
b) Simulated waveforms of switching pulses for phase A
c) Experimental waveforms of switching pulses for phase A
the modulation index for the unfiltered output line-to-line voltage. This illustrates that the THD is inversely proportional to the modulation index $M_i$. In other words, a lower THD in the output voltage is experienced at higher modulation index.

The frequency spectrum of the unfiltered line-to-line voltage captured via YOKOGAWA WT 1800 precision power analyser is shown in Fig. 8b. The graph contains the fundamental component and an infinite number of odd harmonics. Owing to the symmetry attained in the inverter output line-to-line voltage, all even sub-carrier harmonics were eliminated. As it is well known in the PWM signal frequency spectrum, some harmonics are centralised around the carrier frequency ($f_c = 2000$ Hz).

For modulation index $M_i = 0.8$, the THD of the voltage waveform was found to be 25.609%. As depicted in Fig. 8a, this value corresponds very well with the one obtained from the simulation at the same modulation index.

There is another possibility to reach an output voltage with higher number of steps in cascaded multilevel inverters by making a binary (power of two) relationship between the DC-link voltages. Unfortunately, the employment of this strategy in the proposed configuration creates a great difference in power distribution in the inverter cells. Because of this power distribution problem, the inverter needs to be redesigned with different switch technologies like integrated gate commutated thyristor for high power cells, high-voltage IGBT for medium-power cells and low-voltage IGBT for low-power cells. The different semiconductor switches in the same power circuit reduce the inverter modularity, and limits appear in terms of switching frequency and modulation index.

Providing a number of 300-V DC sources with three basic units in (Fig. 1) per inverter leg. In this case 18 switches are used and a number of 300-V DC supplies need to be connected in series in the second and third cells. Table 4

---

**Fig. 4** Figure showing

a Control block diagram

b Prototype of the proposed multilevel inverter
compares the power component requirements and the inverter output voltage between the two different methods that are followed to determine the value of DC supplies for the introduced three-phase multilevel inverter. In the first method, relationship between the DC-link voltages is binary, whereas the second method selects the DC supplies as described in Section 2.

From the above table, it is observed that the first technique brought higher voltage with larger number of steps. Unfortunately, extra DC supplies are required and the switching devices in the third cell are subjected to high voltage. Therefore the use of this method necessitates different switches for high voltage blockage. Since the voltage standing on switches is lower, the deployed method to determine the value of the utilised DC supplies manages to maintain similar switches with an acceptable number of voltage steps. Therefore better modularity is achieved compared to other asymmetrical cascaded configurations.

5 Comparison of the proposed topology with conventional multilevel inverters

For the same number of output voltage steps, Table 5 provides a brief comparison between conventional three-phase
cascaded multilevel inverters and suggested inverter with regard to power component requirements.

The diode clamped multilevel inverter is an attractive high-voltage multilevel inverter because of its robustness [33]. The deviating voltage at the neutral point remains always a distracting feature in NPC inverter. Therefore DC-link capacitor voltage balancing is the crucial task in such configuration [34].

The FC multilevel converter makes use of FCs for voltage clamping [35]. To some extent, these topologies are advantageous. This is due to the less operation performed by the transformer and redundant phase leg states that makes the semiconductor switches share the same distributed stress [36]. The main drawback in such converters is the excessive number of storage capacitors for higher voltage steps. Table 6 provides a comparison between the suggested inverter and the well-known four-level inverters: diode-clamped and FC.

Table 3 11-level inverter requirement based on [23] and the proposed topology

<table>
<thead>
<tr>
<th></th>
<th>Number of voltage levels</th>
<th>Number of utilised switches</th>
<th>Number by utilising DC supplies</th>
</tr>
</thead>
<tbody>
<tr>
<td>the proposed inverter in [23]</td>
<td>11</td>
<td>42</td>
<td>5</td>
</tr>
<tr>
<td>the proposed inverter</td>
<td>11</td>
<td>24</td>
<td>4</td>
</tr>
</tbody>
</table>

The Institution of Engineering and Technology 2013
6 Power losses and inverter efficiency

Power loss is an important index for cost estimation and cooling system design in multilevel inverters. In general, there are two types of semiconductor losses in multilevel inverter configurations. The conduction loss is due to the voltage drop across the active semiconductor device when conducting current. The switching loss occurs at each current commutation of the device and it is directly related to the switching frequency. Other losses like snubber and off state losses are disregarded, since IGBTs (SSNE 0800M170100) were used with negligibly small leakage current during the off state [37].

MATLAB/Simulink model of the proposed 400 KW four-level inverter was developed to study the conduction and switching power losses at different operating conditions. The inverter delivers variable power to a distribution power system. The output of the inverter was connected to the 25 kV, 40 MVA, 50 Hz system through a 2200 V/25 kV transformer. Each leg of the inverter was fed with constant DC supplies $E = 1100$ V and $2E = 2200$ V. The maximum ratings of the selected IGBTs (SSNE 0800M170100) are: forward current of 800 A and a direct voltage of 1700 V.

Conduction losses $P_{\text{cond,IGBT}}$ of IGBT are approximated based on its forward voltage drop, $V_{\text{on,IGBT}}$ and the instantaneous current $I(t)$

$$P_{\text{cond,IGBT}} = \frac{1}{T} \int_{0}^{T} V_{\text{on,IGBT}} I(t) \, dt$$

(11)

Similarly, the conduction loss in a diode can be modelled as

$$P_{\text{cond-d}}(t) = i_D(t) \cdot (V_{\text{fD}} + R_F \cdot i_D(t))$$

(12)

where $V_{\text{fD}}$ is the forward voltage drop across the diode when the forward current of the device $i_D$ draw near zero and $R_F$ is the diode approximate on-state resistance slope.

### Table 4 Comparison between the two methods followed to determine the value of DC supplies for the introduced inverter

<table>
<thead>
<tr>
<th></th>
<th>Binary</th>
<th>Proposed method</th>
</tr>
</thead>
<tbody>
<tr>
<td>number of utilised switches</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>number of utilised DC source (300 V units)</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>number of steps</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>third cell voltage</td>
<td>1200</td>
<td>900</td>
</tr>
<tr>
<td>maximum output voltage</td>
<td>8400</td>
<td>6600</td>
</tr>
<tr>
<td>similarity of switches</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Table 5 Comparison of power component requirements among conventional cascaded multilevel and the proposed topology

<table>
<thead>
<tr>
<th></th>
<th>Symmetrical</th>
<th>Asymmetrical</th>
<th>Proposed topology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Binary</td>
<td>Trinary</td>
<td></td>
</tr>
<tr>
<td>maximum output voltage</td>
<td>E(N_{\text{step}} − 1)/2</td>
<td>E(N_{\text{step}} − 1)/2</td>
<td>E(N_{\text{step}} − 1)/2</td>
</tr>
<tr>
<td>number of utilised switches $M$</td>
<td>6(N_{\text{step}} − 1)</td>
<td>12([ln(N_{\text{step}} + 1)/ln2) − 1]</td>
<td>(12N_{\text{step}}/ln3)</td>
</tr>
<tr>
<td>maximum voltage standing on the switches</td>
<td>6E(N_{\text{step}} − 1)</td>
<td>6E(N_{\text{step}} − 1)</td>
<td>6E(N_{\text{step}} − 1)</td>
</tr>
</tbody>
</table>

For an IGBT with an anti-parallel freewheeling diode, the switching loss can be modelled by the switching loss energy associated with each switching event. In the device datasheet, the switching loss energies, $E_{\text{on}}$ and $E_{\text{off}}$, were established by integrating the product of the collector current characteristic and the collector–emitter voltage characteristic across the total switching time. Over an interval $T$, the average switching power losses in an IGBT module and turn off power loss for the diode are estimated [38].

$$\bar{P}_{\text{on}} = \frac{1}{T} \int_{0}^{T} E_{\text{on}}(t) \, dt$$

(13)

$$\bar{P}_{\text{off}} = \frac{1}{T} \int_{0}^{T} E_{\text{off}}(t) \, dt$$

(14)

$$\bar{P}_{\text{off,d}} = \frac{1}{T} \int_{0}^{T} E_{\text{off,d}}(t) \, dt$$

(15)

Once the total semiconductor losses $P_{\text{loss}}$ in the introduced inverter are defined, the relative efficiency is determined based on the following formula.

$$\text{Efficiency(\%) } = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\%$$

(16)

For 1 KHz carrier frequency with 350 KW output power at a power factor $PF = 0.75$, Fig. 9a depicts the power loss distribution among the switching devices in phase (A) of the proposed inverter. $D_1$, $D_2$, $D_3$ and $D_4$ are the freewheeling diodes with built-in switches $S_1$, $S_2$, $S_3$ and $S_4$, respectively.

In Fig. 9b the inverter efficiencies were calculated at four different power factors. The inverter output power was set to 350 and 250 KW. An improved power factor is achieved by enhancing real power flow transfer. Therefore inverter efficiency varies proportionally and linearly with respect to power factor.

For $P_{\text{out}} = 350$ KW and by considering a typical operating power factor of a transmission line, $PF = 0.75$. The inverter efficiencies at the corresponding five switching frequencies are shown in Fig. 9c. The efficiency varies inversely with
the switching frequency. As the switching frequency increases, the efficiency of the inverter decreases as a result of switching loss being considerably increased in the semiconductor components.

7 Conclusions

A novel topology of three-phase cascaded multilevel inverter was introduced and the suggested configuration came with reduced number of switches and gate driver circuits. The voltage standing on switches is minimised for realising $N$ steps. Therefore the proposed topology results in reduction of installation area and cost. Low-frequency and sinusoidal PWM techniques were comfortably employed and both techniques showed high flexibility and simplicity in control.

Furthermore, the method employed to determine the magnitudes of the DC voltage sources was well executed. In order to verify the performance of the proposed multilevel inverter, a four-level configuration was simulated and its prototype was manufactured.

Fig. 9  Figure showing

\(a\) Power loss distribution among the switching devices in phase (A)

\(b\) Inverter efficiency at different power factors

\(c\) Inverter efficiency at different switching frequencies
The obtained simulation and hardware results met the desired output, and it should be noted that the proposed topology is made for three-phase three-wire load applications. Hence, subsequent work in the future may include an extension to four-wire loads with other different control techniques.

8 Acknowledgment

The authors would like to thank the Ministry of Higher Education of Malaysia and University of Malaya for providing financial support under the research grant no. UM.C/HIR/MEH/ENG/16001-00-D000017.

9 References

36 Mekhilef, S., Khudhur, H.I., Belkamel, H.: ‘DC link capacitor voltage balancing in three level neutral point clamped inverter’. 2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), 2012, pp. 1–4