Digital Control of Three Phase Three-Stage Hybrid Multilevel Inverter

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Abstract—Three-stage 18-level hybrid inverter design with novel control method is presented. The inverter consists of main high-, medium-, and low-voltage stages connected in series from the output side. The high-voltage stage is a three-phase, six-switch conventional subinverter. The medium- and low-voltage stages are made of three-level subinverters constructed by H-bridge units. The proposed control strategy assumes a reference input voltage vector and aims to approximate it to the nearest inverter vector. The control concept is based on holding the high-voltage state as long as it is feasible to do so. The reference voltage vector has been represented in a 60°-spaced two axis coordinate system to reduce the computational effort. The concept of the staged-control has been presented, the transformed inverter vectors and their relation to the switching variables have been defined, and the implementation process has been described. The test results verify the effectiveness of the proposed strategy in terms of computational efficiency as well as the capability of the inverter to produce very low distorted voltage with low switching losses.

Index Terms—Digital control, extended space vector transformation, multilevel converters, pulse width modulation (PWM), space vector modulation (SVM), three-stage hybrid topology, voltage source inverters (VSI).

I. INTRODUCTION

In general, multilevel inverters (MLIs) refer to the class of inverters with output points which have more than two voltage levels with respect to a reference point [1]–[5]. The capacity to produce output voltage levels higher than those of the power semiconductor switching device’s ratings and the reduced distortion and dv/dt stress are the basic MLIs advantages [6], [7]. In addition to the circuit complexity, cost and control difficulty are the main barriers on the MLI expansion road [8]. With the basic MLI topologies, the number of inverter levels is linearly proportional to the number of inverter’s switching devices and this limits the practical number of levels to few levels [9]. Inverter with extended number of levels have been built using the asymmetrical MLI structure, where the inverter’s cascaded H-bridges have been supplied with different voltage levels [10], [11].

Asymmetrical MLI suffers from the need for large number of isolated dc supplies. In order to ease this problem the hybrid MLI structures have been introduced, where the cascaded inverter stages are made of different types of inverters [12]–[16]. Many studies have addressed some issues on MLI control strategies. Most of the proposed control methods are the extension of the conventional inverter control methods for example the multicarrier pulse width modulation (PWM) strategy [17] and multilevel space vector modulation (SVM) control [18]–[21]. The low switching frequency strategies are advantageous as the harmonics distortion is considerably less than the conventional inverters case. Selected harmonics elimination [22] and voltage approximation [23] are examples of the low frequency strategies. On the other hand, some researchers have started developing control strategies which are fundamentally developed for MLI; examples for this are the one dimension [24] and the hybrid modulation [25]. Other works in [26] and [27] also utilized similar topologies and control scheme.

Selecting the dc voltages of the multiple stage inverters in a way that eliminates the voltage level redundancy, or provides exactly one switching combination for each voltage level provides the advantage of maximizing the number of levels can be achieved from the inverter circuit. When the cascaded stages dc voltages are related by a ratio of three, the maximum number of steps is achieved with symmetrical step size [23]. This design, however, has some reservations in control where the high frequency PWM control implies carrier frequency switching of the high-voltage stage simultaneous switching which is to practically unacceptable. Study of the appropriate voltage ratio shows that the modulation condition required to avoid high frequency operation at high-voltage stage is satisfied if any two adjacent voltage levels can be achieved by switching the lowest voltage cells only [26]. This condition is not satisfied with ratio-3 related dc sources, and hence this selection is not appropriate for PWM control. This ratio, however, has been followed by some designs which do not apply PWM control [22]–[35]. Alternatively, the control method followed is to approximate the reference voltage vector to the nearest inverter vector. Whilst determining the nearest inverter vector to the reference vector is systematic, relating this vector a one inverter switching state is not so. The large number of inverter levels results in many switching states sharing the same voltage vector, when a given inverter vector is selected a second stage of processing need to be included to determine which switching state related to this vector is going to be applied. This option has not been utilized in previous research applying voltage approximation of inverters with...
a large number of stages [22], [23]. On the other hand asymmetrical MLI, which results from supplying the CHB cells with different dc voltages, provides higher number of levels for the same circuit topology [27]–[30].

The study presented in [27] have suggested a stage-by-stage vector control structure to mitigate the problem of switching state selection among the extended number of equivalent states. The available flexibility is utilized to minimize the switching actions giving the priority in this to the higher voltage stage. This paper applies the same structure but proposes a simplified and efficient control technique based on the transformed reference and inverter voltage vectors.

The hybrid MLI circuit treated herein and its switching variables definition are given in Section II. The control concept is introduced in Section III. Section IV introduces the proposed control technique. In Section V, the test results are presented. The control execution time is compared to the basic implementation presented by other authors.

II. MULTILEVEL INVERTER TOPOLOGY AND SWITCHING STATES

A. Inverter Circuit Topology

The inverter circuit shown in Fig. 1 consists of the “main” high voltage six-switch inverter, with each output line connected in series to form two cascaded single-phase full bridge inverters. The main and H-bridge cells are fed by isolated dc sources of 9, 3, and 1 Vs where Vs is the per unit dc source. In this design, the high-voltage stage has only one dc source operates with reduced current ripple compared to the three dc sources of the cascaded H-bridge design providing considerable reduction in the dc source cost and losses.

With respect to the negative terminal of the 9-Vs dc voltage source, the output points (A, B, and C) have voltage ranges between maximum of \((9 + 3 + 1)\) Vs = 13 Vs, and minimum of \((0 - 3 - 1)\) Vs = -4 Vs, with uniform voltage step of Vs, therefore the cascaded inverter of Fig. 1 forms an 18-level inverter.

![Fig. 1. 18 level inverter topology.](image)

Using (1), the voltage vector of any inverter state can be achieved. Alternatively, the voltage vector diagram of the three-stage inverter is drawn by two superposition steps. First, the vector diagram of the three-level medium-voltage stage inverter (composed of 19 vectors) is drawn at the end of each of the seven vectors of the high-voltage stage. Then, the vector diagram corresponding to low-voltage stage has been super-imposed at the ends of resultant vectors as shown in Fig. 2.

![Fig. 2. Voltage vectors of the 18-level inverter as the sum of the three cascaded inverters vectors.](image)

B. Voltage Vectors and Inverter States

The switching variables of the inverter are denoted by \(\{(x_{ABC}), (y_{ABC}), (z_{ABC})\}\) where \(x\) is a binary digit while \(y\) and \(z\) are trinary digits. The states of the high-, medium-, and low-voltage stages are determined by \(x_{ABC}\), \(y_{ABC}\), and \(z_{ABC}\), respectively. The output voltage vector can be represented in terms of the switching state as shown in (1) [27]

\[
\begin{bmatrix}
x_d \\
y_d
\end{bmatrix} - V_s \begin{bmatrix}
1 & -0.5 & -0.5 & -0.5 \\
\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix} \begin{bmatrix}
x_A + 3y_A + z_A \\
x_B + 3y_B + z_B \\
x_C + 3y_C + z_C
\end{bmatrix}. \tag{1}
\]

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18-level inverter vectors can be represented by more than one combination of the three stages voltage vectors. For example vector V1 shown in Fig. 2 is represented as $V_{1H} + V_{1M} + V_{1L}$ once and next as $V_{1H'} + V_{1M'} + V_{1L'}$, where $V_{1H}$, $V_{1M}$ and $V_{1L}$ are the voltage vectors corresponding to high, medium, and low voltage inverter cascaded stages, respectively.

It is highly desirable for the switching frequency of the high-voltage stage to be reduced as mentioned in [27]. The control concept explained in this section aims to hold the high voltage vector as long as the reference vector can be represented by adding other medium and low vectors to this high voltage vector shall refer to the hexagonal area marked by the vectors reachable through a given high state vector by its “domain.” The seven domains of the high-voltage stage vectors are depicted in Fig. 3.

Dividing the space vectors area into domains is extended to the middle stage vectors. Nineteen hexagons, each represents the area covered by low-voltage stage vector diagram, can be drawn within each of the seven high state domains at the tips of the 19 medium voltage vectors. For illustration, one of the middle state domains hexagons is shown in Fig. 3. With $x_{abc} = 100$ and $y_{h:v} = 200$, the low-voltage stage selection will cover the small hexagon marked at the rightmost side of Fig. 3, we shall refer to it as the domain of state [100, 200].

Within the inverter vector space some of the regions are covered by exactly one high state domain without overlap. If the reference vector is located in such area, the system controller should select the corresponding high state. Other areas are covered by two- or three-high state domains; in this case there is more than one option in the selection of $x_{ABCD}$. We have exploited this to minimize the switching actions at the higher voltage stages. The medium state domains also overlap and this will be able to be utilized in similar way.

**B. Controller Structure**

To realize the control concept the control structure shown in Fig. 4 is developed by the authors. The cascaded structure designs have similar control procedure for the high and medium stages. In these stages the reference vector is compared to the present state domain, if the reference vector is located in this domain the present state holds for the following sampling cycle. Otherwise, the reference vector sector and zone are determined. The zone definition has been introduced to specify the reference vector location with respect to the domains overlap. Therefore, by defining the zone each domain under which the reference vector is located will be specified. Then, the present state is also taken into account to select the next inverter stage state.

The low-voltage stage controller identifies one inverter vector as the nearest one to the reference vector. If this vector is associated with more than one inverter switching state, the state nearest to the present state will be chosen.

In [27], the above calculations processing were carried out in the $d$-$q$ space system and the calculation process included floating point calculations with several if-then trees for reference vector zone determinations. In Section III an axis transformation is introduced to simplify the calculation process.
For control algorithm implementation, the controller card “ezdsp F2818” based on the TMS320F2812 DSP has been selected.

IV. VOLTAGE VECTOR APPROXIMATION IN $g$–$h$ AXIS SYSTEM

The 60°-spaced $g$–$h$ coordinate system shown in Fig. 5 will be used to represent the voltage vector in the proposed control algorithm. This control system allows simpler and faster calculations compared to the basic $d$–$q$ space system as it is tightly related to the inverter states voltage vectors. Fig. 6 shows that the voltage vectors of two- and three-level hybrid stages inverter have $g$–$h$ coordinates which are ($\pm 1$, $0$) multiples of the dc source voltage for the two-level stage and ($\pm 2$, $\pm 1$, $0$) multiples of the dc source voltage for the three-level stages. The integer coordinates of the inverter vectors allow the inverter control by simple fixed-point calculations.

A. Control Algorithm in $g$–$h$ Axes System

The next switching state is determined as illustrated in control algorithm flow diagram shown in Fig. 7. The control process starts with $d$–$q$ to $g$–$h$ axis transformation of the sampled reference vector. Equations (2) and (3) are used for vector transformation

$$
g_{\text{ref}} = |V_{\text{ref}}| \times \left( \cos \theta_{\text{ref}} - \frac{\sin \theta_{\text{ref}}}{\sqrt{3}} \right) \quad (2)
$$

$$
h_{\text{ref}} = |V_{\text{ref}}| \times \left( \frac{2 \sin \theta_{\text{ref}}}{\sqrt{3}} \right) \quad (3)
$$

where $|V_{\text{ref}}|$ and $\theta_{\text{ref}}$ are the reference voltage vector amplitude and angle.

The calculation of $x_{ABC}$ is done by the determination if the reference vector is located in the domain of the current high-voltage state. If so, $x_{ABC}$ holds its value during the next switching interval. Otherwise the nearest high-voltage state is determined by comparing the reference to the seven high state domains and creating a feasible next state list. If this list has more than one element reflecting that the reference vector is located in domains overlap, the controller selects $x_{ABC}$ which is nearer one to the initial value.

The middle reference is calculated by subtracting the voltage vector corresponding to the next $x_{ABC}$ from the input reference voltage vector. The medium stage controller is similar to the high-voltage stage controller except for the size of the domain and the number of vectors of the three stages inverter is 19 rather than seven.

Indeed the calculations described above are far simpler than the calculations presented in [27] due to the integer dimensions of the inverter vectors and the straightforward relationship between the inverter $g$–$h$ dimension and its switching state (4) and (5)

$$
\begin{bmatrix}
  v_g \\
  v_h
\end{bmatrix} = gV_s \begin{bmatrix}
  1 & -1 & 0 \\
  0 & 1 & -1
\end{bmatrix} \begin{bmatrix}
  x_A \\
  x_B \\
  x_C
\end{bmatrix}. \quad (4)
$$

For high-voltage stage

$$
\begin{bmatrix}
  v_g \\
  v_h
\end{bmatrix} = 3V_s \begin{bmatrix}
  1 & -1 & 0 \\
  0 & 1 & -1
\end{bmatrix} \begin{bmatrix}
  y_A \\
  y_B \\
  y_C
\end{bmatrix}. \quad (5)
$$

for medium-voltage stage. The low-voltage stage switching variables $g$–$h$ vectors relationship is indicated in (6)

$$
\begin{bmatrix}
  v_g \\
  v_h
\end{bmatrix} = V_s \begin{bmatrix}
  1 & -1 & 0 \\
  0 & 1 & -1
\end{bmatrix} \begin{bmatrix}
  z_A \\
  z_B \\
  z_C
\end{bmatrix}. \quad (6)
$$

The reference voltage for the low-voltage stage is determined by subtracting the vector corresponding to the calculated $y_{abc}$ from the medium stage reference vector as shown in Fig. 7.
In (7), the three switching variables \( Z_{ABC} \) are determined (6). The third equation assumes that the three variables add up to zero is considered. The solution of (7) is a linear space of solutions from which one or two specific solutions can be obtained by adding a constant to \( Z_{ABC} \) that sets the minimum to 0 or the maximum to 2. When two solutions obtained, the one nearer to the initial state is selected. The reference voltage vector input is required to be approximated during the following sampling interval. The controller operates the inverter in the state that produces the vector nearest to the reference vector and holds this state during the entire sampling interval.

The solution space is found from (8)

\[
\begin{bmatrix}
  z_A' \\
  z_B' \\
  z_C'
\end{bmatrix} = \frac{1}{3V_s} \begin{bmatrix}
  2 & 1 & \nu_{g,ref} \\
  -1 & 1 & \nu_{h,ref} \\
  -1 & -2 & \nu_{l,ref}
\end{bmatrix}.
\]

The first specific solution is given in (9)

\[
\begin{bmatrix}
  z_A \\
  z_B \\
  z_C
\end{bmatrix} = \begin{bmatrix}
  z_A' \\
  z_B' \\
  z_C'
\end{bmatrix} - \min(z_A', z_B', z_C').
\]

and the second specific solution is given in (10)

\[
\begin{bmatrix}
  z_A \\
  z_B \\
  z_C
\end{bmatrix} = \begin{bmatrix}
  z_A \\
  z_B \\
  z_C
\end{bmatrix} + [2 - \max(z_A', z_B', z_C')].
\]

As in the method presented earlier, there is a close similarity between the high and medium stages calculations. The calculation of \( Z_{ABC} \) begins by the determination if the reference vector is located in the domain of the present high-voltage state. If so, \( Z_{ABC} \) holds its value during the next switching interval. The examination conditions are as follows:

\[
|v_{h,ref} - (x_{A,ini} - x_{C,ini})| 9.8 < 8V_s
\]

and

\[
|v_{g,ref} - (x_{A,ini} - x_{B,ini}) + (v_{h,ref} - (x_{A,ini} - x_{C,ini})| 9.8 < 8V_s
\]

If the conditions given above are not satisfied, the reference vector is located outside the present high-voltage state domain. Hence, a new high-voltage state is determined in two steps. The first step is to generate the feasible next \( x_{ABC} \) vector which is formed by the states that have the reference vector located in their domains or valid candidates as next states. The feasible states vector is basically generated by applying conditions similar to (11) and (12) for all the eight possible \( x_{ABC} \) combinations. The number of iterations can be reduced by excluding one of the zero states, and the present state from the comparison. Also the iteration can be stopped if the number of feasible vectors reached three, which is the maximum number of overlapping high stage domains as shown in Fig. 3. The second step is to compare the feasible next states vector to the current \( x_{ABC,ini} \) and choose the nearest element as the next high-voltage state. As in the q-d based algorithm, the medium reference is determined by subtracting the vector corresponding to the selected high state from the reference vector, as follows:

\[
v_{g,ref,n} = v_{g,ref} - 9(x_A - x_B) V_s
\]

\[
v_{h,ref,n} = v_{h,ref} - 9(x_B - x_C) V_s
\]

If the solution of (10) is different than (9), then the one nearer to the initial state is selected. In voltage approximation using standard \( q-h \) transformation, the next switching state is determined as illustrated in the flow diagram shown in Fig. 7. In other words, this process is carried out in three consecutive stages: the high, medium, and low stages. Each stage considers its previous output in the calculation of its new state. The previous output is
provided by the memory blocks \( Z^{-1} \). The process starts with the \( d-q \) to \( g-h \) reference coordinate transformation according to the (4), (5), and (6) for high, medium, and low stages.

Inverter vectors coordinates are also integers range between \(-2\) and \(-2\) multiplied by the stage dc voltage which is denoted by \( V_{dc} \). The integer coordinates of the inverter vectors allow the inverter control to be completed with simple fixed point calculations. The \( g-h \) coordinates of any subinverter voltage vector as a function of the switching variable are given by

\[
\begin{bmatrix}
V_g \\
V_h
\end{bmatrix} = V_{dc} \begin{bmatrix}
1 & -1 & 0 \\
0 & 1 & -1
\end{bmatrix} \begin{bmatrix}
V_A \\
V_B \\
V_C
\end{bmatrix}.
\] (15)

Equation (15) is applicable for all the three inverter stages after substituting the corresponding dc voltage and switching variables. Reference voltage vector input is required to be approximated during the following sampling interval. The controller operates the inverter in the state that produces the vector nearest to the reference vector and holds this state during the entire sampling interval. In voltage approximation using \( g-h \) transformation, the next switching state is determined as illustrated in the flow diagram shown in Fig. 7.

V. TESTING RESULTS AND DISCUSSION

A. Experimental Setup

The control algorithm has been implemented using DSP controller board eZdsp F2812. The 150 MHz, fixed point, low cost CPU, executed the algorithm with a sampling frequency exceeding 45 kHz and using the on-chip memory only, this reflects the computational efficiency of the proposed algorithm.

A prototype of the proposed inverter has been built and tested as shown in Figs. 8 and 9. The low- and medium-voltage stages have been supplied by a lead acid 12 V–5.5 Ah batteries. Three series connected units are used for the medium-voltage stage to supply 36 V. The high-voltage stage has been fed by the laboratory dc power supply. For high and medium-voltage stages, IGBTs are used, while MOSFETs have been used for the low-voltage stage. A 1 kW motor has been supplied by the inverter to act as a load. Picture and block diagram of the proposed experimental set up at Industrial Electronics Research Laboratory at University Malaya is provided. Also the screenshots from the experimental data obtained and results for observing reference voltage 100%, 80%, 70%, 50%, 40%, and 10% are provided.

B. Measured Results

Fig. 10 shows the experimental measured phase voltage waveforms for different values of the reference amplitude. The inverter voltage quality is affected at very low reference amplitude due to the reduction in the number of steps. However, conducting several experiments with a reference input of 40% or higher, the output voltage THD is less than 4.5%. Fig. 11 shows the variations in number of levels and harmonic distortions against the reference amplitudes.

C. Discussions

The results show that the proposed algorithm is equivalent in its operation to that proposed in [27] in terms of resultant switching signals and output line to line voltage. This is well expected as the two algorithms were built on the same control concept. The transformation technique, however, saves about 50% of the computation time as the maximum sampling frequency achieved in [27] is about 25 kHz. In addition a comparison between the proposed topology and [14] is shown in Table I.

The proposed control algorithms can be used on the basis of a dual control method that controls the low-voltage stage in PWM mode, and in this case, the resultant system will be unique in combining the high frequency control with the state redundancy elimination.
**D. Computationally Efficient Control**

By the staged structure of the controller, a great deal of computational effort has been saved.

In the voltage approximation using basic $d-q$ axis calculations, many options have been applied to reduce the computational effort, for example, implying the sector of the reference angle in the angle coding system and determining the low state zone using single sum of integer product step. Additionally the polynomial-based calculations of the low-voltage stage gives the reference zone in one fixed-point sum-of-products term with all product terms except one are zeros.

The computational efficiency of the voltage approximation control has been greatly improved by applying the $g-h$-based
calculation concept and the required memory has been considerably reduced. The high and medium stages calculations have been made using pure integer calculations, and the developed low-voltage stage calculations avoids the axis transformation step that would be required if the polynomial low state zone identification is used.

VI. CONCLUSIONS

A three-stage hybrid 18-level inverter and its innovated control strategy have been presented in this paper which consists of three stages of two and three-level inverters. The multilevel topology saves the cost of the dc source. Asymmetrical dc supplies ratio maximizes the number of levels.

The suggested strategy exploits the inverter’s high resolution to approximate any reference vector by one inverter vectors. With the integer calculations allowed by introduced vector transformation, the control digital algorithm has been tested using low memory fixed point low cost processor. This processor runs the control algorithm with speed which is satisfactory for most applications.

The experimental results showed that the output voltage waveform had very small harmonic distortion for wide range of reference magnitudes. This eliminates the need for added output filter.

The high-voltage stage inverter operates in the square wave mode. The medium-voltage stage operates at a few multiples of the fundamental frequency. The proposed control method could be extended to PWM control mode by applying PWM control on the low-voltage stage and the proposed control method on higher voltage stages.

REFERENCES


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