Russell Tessier

Curriculum Vitae

University of Massachusetts
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Research Interests

My research interests are in the areas of field-programmable architectures, VLSI, and high-performance and parallel computer architecture. I am particularly interested in the integration of these fields to support embedded systems.

Education

Massachusetts Institute of Technology ..... Cambridge, MA

Ph.D.	Electrical Engineering and Computer Science	1999
S.M.	Electrical Engineering and Computer Science	1992

Rensselaer Polytechnic Institute ..... Troy, NY

B.S.	Computer and Systems Engineering	1989

Current Research

University of Massachusetts ..... Amherst, MA

1/99 – present

I am currently the head of the UMass Reconfigurable Computing Group. This research effort involves six students. Current research topics include: reconfigurable architectures, embedded system security and fault tolerance, and embedded applications, such as radar processing and virtual networking.

Other Research Experience

Université de Bretagne Sud ..... Lorient, France

6/07 – 7/07
5/08 – 6/08
6/11 – 7/11

Visiting Researcher – I assisted Prof. Guy Gogniat in developing new security protocols for FPGA-based embedded systems.

University of Toronto ..... Toronto, ON, Canada

1/05 – 12/05

Visiting Researcher – I assisted Prof. Jonathan Rose in developing new FPGA architectures and CAD algorithms during a one-year sabbatical appointment.

CASA Engineering Research Center - UMass ..... Amherst, MA

10/03 – 12/06

Project Leader – I supervised the development and implementation of an FPGA-based digital acquisition system which is an integral part of a weather sensing system. To date, five weather radar systems which include the data acquisition system have been deployed in Oklahoma and Massachusetts. The systems are currently being used in weather prediction and tornado detection.

Massachusetts Institute of Technology ..... Cambridge, MA

12/93 – 10/98

Fast Floorplanning and Routing Algorithms – My doctoral thesis examined algorithmic techniques to reduce place and route time for large field programmable gate arrays (FPGAs). To support this work, I implemented an FPGA layout system called *Frontier* that rapidly evaluates place and route tradeoffs for hierarchical RTL designs. Advisor: Steven Ward.

11/92 – 12/93

Virtual Wires Logic Emulation – I designed and implemented the hardware for an FPGA-based logic emulation system. This scalable system uses an inter-FPGA communication protocol based on static scheduling to overcome limited device pin resources. The hardware and software for this project were later commercialized by Virtual Machine Works.

1/90 – 10/92 NuMesh Parallel Processing – I was a member of the NuMesh group, which worked to design, implement, and explore statically-scheduled multiprocessor routing. My specific contributions to this research included the specification of a hardware communication protocol and the design and implementation of a Sparc-based processing element, high-speed frame buffer, and host computer interface card.

Rensselaer Polytechnic Institute ..... Troy, NY

9/88 – 5/89 Image Processing – I designed an analog signal acquisition board for an ultrasound imaging system.

Teaching Experience

University of Massachusetts ..... Amherst, MA

9/04 – Present Associate Professor of Electrical and Computer Engineering. Course instructor for *Data Structures*, *Introduction to Electrical and Computer Engineering II*, *Reconfigurable Computing*, *Senior Design Project*, and *Parallel Computer Architecture*.

1/99 – 8/04 Assistant Professor of Electrical and Computer Engineering. Course instructor for *Introduction to Electrical and Computer Engineering*, *Computer Systems Laboratory II*, *Reconfigurable Computing*, and *Parallel Computer Architecture*.

University of Toronto ..... Toronto, ON

9/05 – 12/05 Visiting Professor of Electrical and Computer Engineering. Course instructor for *Reconfigurable Computing*.

Massachusetts Institute of Technology ..... Cambridge, MA

5/93 – 12/97 Junior faculty instructor for *Computation Structures*

9/89 – 5/92 Teaching assistant for *Parallel Processing*, *Microcomputer Project Laboratory*, *Dynamic System Control*, and *Computation Structures*

Professional Experience

Mentor Graphics (formerly Ikos Systems) ..... Waltham, MA

5/96 - 9/01
11/08 – 1/09 *Systems Design Consultant*. Involved in the design, implementation, and evaluation of FPGA-based logic emulation systems. Hardware design and FPGA evaluation were important aspects of the job.

Altera Corporation ..... Toronto, ON

1/05 - 9/05 *Software Engineer*. Developed power-aware computer-aided design algorithms for FPGA embedded memory mapping and logic block placement.

Prosensing, Inc. ..... Amherst, MA

9/00 - 1/04 *Hardware Design Consultant*. Assisted in the development and debug of digital data acquisition systems.

Altera Corporation ..... San Jose, CA

10/01 - 4/02 *Consultant*. Expert witness in a civil lawsuit.

Virtual Machine Works ..... Cambridge, MA

1/94 - 5/96 *Founder and Principal Engineer*. One of three founders of a logic emulation company based on research performed at MIT. I aided in the design and development of FPGA-based emulation hardware. The company was acquired by Ikos Systems in May 1996.

BBN Corporation ..... Cambridge, MA

6/92 - 1/94 *Hardware Engineer*. Designed a multiprocessing node for a satellite land station. I performed all component selection, schematic entry, and verification for the design.

Data General Corporation ..... Westboro, MA

5/89 - 8/89 *Software Engineer*. Assisted in the development of a debugging tool for a RISC-based, fault-tolerant computer system.

Patents

Russell Tessier, Vaughn Betz, Thiagaraja Golpalsamy, and David Neto, "Power-Aware RAM Processing." U.S. patent 7877555, January 25, 2011.

Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5761484, June 2, 1998.

Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5596742, January 21, 1997.

Service

Co-Editor, special issue: EURASIP Journal of Embedded Systems, 2006
Co-Editor, special issue: Journal of VLSI Signal Processing, January 2004
Advisor, Eta Kappa Nu student chapter, University of Massachusetts, Amherst, 2003 - 2004, 2006 - 2008
Co-General Chair, FCCM'2010
Co-Program Chair, FCCM'2009
Program Committee, FCCM'2007 - 2011
Finance Chair, FPGA'2005
General Chair, FPGA'2004
Program Chair, FPGA'2003
Publicity Chair, FPGA'2001, FPGA'2002
Program Committee, FPGA'2000 - 2005, FPGA'2007 - 2011
Co-Program Chair, FPT'2011
Program Committee, FPT'2002 - 2011
Program Committee, FPL'2006 - 2007, FPL'2009 - 2011
Program Committee, ARC'2004 - 2008
Special Sessions Chair, ICCD'2011
Panelist for the National Science Foundation, 2002, 2005, 2009, 2010
Chair, IEEE Springfield Chapter, 2000 - 2003
Reviewer for various IEEE and ACM journals and conferences

Awards

Keynote address, Conference on the Engineering of Reconfigurable Systems and Algorithms, 2010
UMass Distinguished Teaching Award, nominee, 2010
Keynote address, Conference on Reconfigurable Communication-Centric SoCs, 2007
Early Tenure and Promotion, University of Massachusetts, 2004
UMass College of Engineering Outstanding Junior Faculty Award, 2002 - 2003
UMass College of Engineering Outstanding Teaching Award, 2002 - 2003
Lilly Teaching Fellow, 2002 - 2003
IEEE Student Chapter Outstanding Faculty Award, 2001

Funded Proposals

Securing the Router Infrastructure of the Internet (co-PI, PI T. Wolf)
Funding source: National Science Foundation 9/1/11-8/31/14
Amount: $500,000

Migration of the DE4 to the NetFPGA (sole-PI)
Funding source: Altera Corporation 9/1/10-12/31/12
Amount: $45,000

On-Chip Sensing Strategies for Efficient Scalability in Many-Core Architectures (PI, co-PI W. Burleson)
Funding source: Semiconductor Research Corporation 8/1/10-7/31/13
Amount: $300,000

Automated Counting of Pedestrians and Bicyclists on an Urban Roadside (PI, co-PI D. Ni)
Funding source: MassHighway 10/1/09-12/31/11
Amount: $228,000

Vehicle Infrastructure Integration (VII): Exploring the Application of Disruptive Technology to Assist Older Drivers (co-PI, PI: D. Ni)
Funding source: New England University Transportation Consortium 9/1/09-12/31/10
Amount: $100,000

Reconfigurable, Next-Generation Network Monitoring (PI, co-PI: T. Wolf)
Funding source: Altera Corporation 9/1/09-12/31/11
Amount: $25,000

Low-Power High Bandwidth Receiver for Ka-Band Interferometry (co-PI, PI: P. Siqueira)
Funding source: NASA 3/1/09-2/28/12
Amount: $1,088,000

Network Virtualization Using Dynamic FPGA Reconfiguration (PI, co-PI: L. Gao)
Funding source: National Science Foundation 9/1/08-8/31/12
Amount: $350,000

CRI: CAD Tool and Compiler Repository for Reconfigurable Computing (sole-PI)
Funding source: National Science Foundation 8/1/07-7/31/11
Amount: $157,500

MNOC: A Network-on-Chip for Configurable Monitors (co-PI, PI: W. Burleson)
Funding source: Semiconductor Research Corporation 4/1/07-1/31/10
Amount: $300,000

X-Band IC Technologies for Low Cost Radars (co-PI, PI: R. Jackson)
Funding source: Raytheon Corporation 4/1/07-1/31/09
Amount: $400,000

FPGA-Based Image Processing Research (co-PI, PI: P. Kelly)
Funding source: Kollmorgen Corporation 1/1/07-1/01/08
Amount: $77,000

Scalable Parallel Processing Using Soft Multiprocessors (sole-PI)
Funding source: Altera Corporation 8/1/06-12/31/07
Amount: $25,000

Power Consumption Comparison for FPGAs and Microprocessors (sole-PI)
Funding source: ST Microelectronics 8/1/04-12/31/06
Amount: $13,000

Power-Aware Logic Synthesis and Tech. Mapping for LUT-based FPGAs (sole-PI)
Funding source: Altera Corporation 1/1/04-12/31/05
Amount: $35,000

CASA Engineering Research Center (Investigator, PI: D. McLaughlin)
Funding source: National Science Foundation 10/1/03-12/31/06
Amount: $200,000

Reconfigurable Implementation of Software Radios (sole-PI)
Funding source: M/A-COM Corporation 1/1/03-12/31/03
Amount: $36,000

Architectures and Technology Mapping Issues for Hybrid FPGAs (sole-PI)
Funding Source: Xilinx Corporation 6/01/01-8/31/02
Amount: $13,200

Integration of JBits and VPR (sole-PI)
Funding Source: Xilinx Corporation 6/01/01-8/31/02
Amount: $10,000

ITR/ACS: Adaptive Fault Recovery for Networked Digital Systems (sole-PI)
Funding Source: National Science Foundation 9/01/00-8/31/03
Amount: $185,000

Low-power Adaptive Systems on a Chip (co-PI, PI: W. Burleson)
Funding source: National Science Foundation 7/1/00-6/31/03
Amount: $300,588

Acquisition of Sensing Data on a Reconfigurable Platform (PI, co-PI: D. McLaughlin)
Funding source: Air Force Research Laboratory 12/1/00-6/31/02
Amount: $69,936

Reconfigurable, Time-aware Smartcard Technology (co-PI, PI: S. Desu)
Funding source: Sharp Corporation 12/1/00-11/31/02
Amount: $200,000

Integration of SystemC with a VirtuaLogic Emulation System (sole-PI)
Funding source: Ikos Systems, Inc. 6/1/00-5/31/01
Amount: $11,771

Reconfigurable Computing with Tiled Architectures (sole-PI)
Funding source: UMass Healey Endowment Grant 5/1/99-5/31/00
Amount: $9,000

Ph.D Degree Thesis Advisees

1. Jia Zhao, "On-Chip Monitoring Infrastructures and Strategies for Multi-core and Many-core Systems", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, January 2012 (expected).
2. Weifeng Xu, "Software Based Permanent Fault Recovery Techniques Using Inherent Hardware Redundancy", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2007.
3. Murali Kudlugi, "Static Scheduling of Multi Domain Circuits for Functional Verification", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2005.
4. Jian Liang, "Development and Verification of a System-on-a-Chip Communication Architecture", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2004.
5. Srini Krishnamoorthy, "Design Mapping Algorithms for Hybrid FPGAs Containing LUTs and PLAs", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2004.

Masters Degree Thesis Advisees

1. Gayatri Prabhu, "Automated Detection and Counting of Pedestrians on an Urban Roadside", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012.
2. Akilesh Krishnamurthy, "Design of an FPGA-based Array Formatter for CASA Phase-Tilt Radar System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012.
3. Vishwas Vijayendra, "Design and Testing of a Prototype High Speed Data Acquisition System for NASA", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, August 2011.
4. Benjamin Bovée, "Simulating a Universal Geocast Scheme for Vehicular Ad Hoc Networks", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2011.
5. Emmanuel Seguin, "Low Cost FPGA Based Digital Beamforming Architecture for CASA Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2010.
6. Salma Mirza, "Scalable, Memory-Intensive Scientific Computing on Field Programmable Gate Arrays", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010.

7. Ramakrishna Vadlamani, "Approaches to Multiprocessor Error Recovery Using an On-Chip Interconnect Subsystem", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010.
8. Deepak Unnikrishnan, "Application-Specific Customization and Scalability of Soft Multiprocessors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2009.
9. Sailaja Madduri, "MNoC: A Network-on-Chip for Monitors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2008.
10. Kevin Andryc, "A Novel Approach to PCI Simulation Using ScriptSim", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2008.
11. Jonathan Allen, "Energy Efficient Adaptive Reed-Solomon Decoding System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2008.
12. David Howland, "RTL Dynamic Power Optimization for FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2007.
13. Kevin Oo Tinmaung, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2006.
14. Rishi Khasgiwale, "Reconfigurable Data Acquisition System for Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005.
15. Lilian Atieno, "Run-Time Dynamically Reconfigurable Reed-Solomon Decoder System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005.
16. Eric Keller, "Programming Model for Network Processing on FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005.
17. David Jasinski, "An Energy-Aware Active Smart-Card Architecture", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003.
18. Ramshankar Ramanarayanan, "Self-Test and Reconfiguration to Support Fault Tolerance in VLIW Processors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003.
19. Arun Ramanathan, "Acquisition of Sensing Data on a Reconfigurable Platform", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2003.
20. Vibhor Garg, "A PCI-X Bus Transactor Model for SOC Verification Using Co-Modeling", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2002.
21. Sriram Swaminathan, "An FPGA Based Adaptive Viterbi Decoder", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001.
22. Ramaswamy Ramaswamy, "Integration of SystemC with an Ikos VirtuaLogic Emulator", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001.
23. Navin Vemuri, "BDD-based Logic Synthesis for LUT-Based FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2001.

Book Chapters

1. Russell Tessier, "Multi-FPGA Systems: Logic Emulation", in Reconfigurable Computing, Scott Hauck and André DeHon, eds., Morgan Kaufmann, pp. 637-670, 2008.
2. Russell Tessier and Wayne Burleson, "Reconfigurable Computing and Digital Signal Processing: Past, Present, and Future", in Programmable Digital Signal Processors, Yu Wen Hu, ed., Marcel Dekker, pp. 147-186, 2002.

Journal Publications

1. Jeŕemie Crenne, Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, and Deepak Unnikrishnan, "Configurable Memory Security in Embedded Systems", accepted/to appear in *ACM Transactions on Embedded Computer Systems*, 25 pages.
2. Jia Zhao, Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson, and Russell Tessier, "A Dedicated Monitoring Infrastructure For Multicore Processors", in *IEEE Transactions on VLSI Systems*, vol. 19, no. 6, pp. 1011-1022, June 2011.
3. Tilman Wolf, Russell Tessier, and Gayatri Prabhu, "Securing the Data Path of Next-Generation Router Systems, in Computer Communications", in *Computer Communications*, vol. 31, no. 4, pp. 598-606, April 2011.
4. Dong Yin, Deepak Unnikrishnan, Yong Liao, Lixin Gao, and Russell Tessier, "Customizing Virtual Networks with Partial FPGA Reconfiguration", in *ACM Computer Communication Review*, vol. 41, no. 1, pp. 125-132, January 2011.
5. Weifeng Xu and Russell Tessier, "Tetris-XL: A Performance-Driven Spill Technique for Embedded VLIW Processors", in *ACM Transactions on Architecture and Code Optimization*, vol. 6, no. 3, pp. 1-40, September 2009.
6. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Edward Wanderley, Russell Tessier and Wayne Burleson, "A Security Approach for Off-Chip Memory in Embedded Microprocessor Systems", in *Journal of Microprocessors and Microsystems*, vol. 33, no. 1, pp. 37-45, February 2009.
7. Ian Kuon, Russell Tessier, and Jonathan Rose, "FPGA Architecture: Survey and Challenges", in *Foundations and Trends in Electronic Design Automation*, vol. 2, no. 2, pp. 135-253, February 2008.
8. Russell Tessier, Vaughn Betz, David Neto, Aaron Egier, and Thiagaraja Gopalsamy, "Power Efficient RAM Mapping Algorithms for FPGA Embedded Memory Blocks", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 2, pp. 278-290, February 2007.
9. Prem Menon, Weifeng Xu, and Russell Tessier, "Design-Specific Path Delay Testing in Lookup Table-based FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 867-877, May 2006.
10. Russell Tessier, David Jasinski, Atul Maheshwari, Aiyappan Natarajan, Weifeng Xu, and Wayne Burleson, "An Energy-Aware Active Smart Card", in *IEEE Transactions on VLSI Systems*, vol. 13, no. 10, pages 1190-1199, October 2005.
11. Russell Tessier, Sriram Swaminathan, Ramaswamy Ramaswamy, Dennis Goeckel, and Wayne Burleson, "A Reconfigurable, Power-Efficient Adaptive Viterbi Decoder", in *IEEE Transactions on VLSI Systems*, vol. 13, no. 4, pages 484-488, April 2005.
12. Jian Liang, Andrew Laffely, Sriram Srinivasan, and Russell Tessier, "An Architecture and Compiler for On-Chip Communication", in *IEEE Transactions on VLSI Systems*, vol. 12, no. 7, pages 711-726, July 2004.
13. Gordon Farquharson, William Junek, Arun Ramanathan, Steven Frasier, Russell Tessier, David McLaughlin, and Mark Sletten, "A Pod-Based Dual-Beam InSAR", in *IEEE Transactions on Geoscience and Remote Sensing*, vol 1, no. 2, pages 62-65, April 2004.
14. Atul Maheshwari, Wayne Burleson, and Russell Tessier, "Trading Off Transient Fault Tolerance and Power Consumption in Deep Submicron VLSI Circuits", in *IEEE Transactions on VLSI Systems*, vol 12, no. 1, pages 299-311, March 2004.

15. Prashant Jain, Andrew Laffely, Wayne Burleson, Russell Tessier, and Dennis Goeckel, "Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations", in *Journal of VLSI Signal Processing*, vol 36, no. 1, pages 27-40, Kluwer Publishers, January 2004.

16. Srini Krishnamoorthy and Russell Tessier, "Technology Mapping Algorithms for Hybrid FPGAs Containing Look-up Tables and PLAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol 22, no. 5, pp. 545-559, May 2003.

17. Ian Harris and Russell Tessier, "Testing and Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.* vol 21, no. 11, pp. 1137-1143, November 2002.

18. Murali Kudlugi and Russell Tessier, "Static Scheduling of Multiple Asynchronous Domains for Fast Functional Verification", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol 21, no. 11, pp. 1253-1268, November 2002.

19. Russell Tessier and Snigdha Jana, "Incremental Compilation for Parallel Logic Verification Systems", *IEEE Transactions on VLSI Systems,* vol 10, no. 5, pp. 623-636, October 2002.

20. Navin Vemuri, Priyank Kalla, and Russell Tessier, "BDD-based Logic Synthesis for FPGAs", in *ACM Transactions on Design Automation of Electronic Systems,* vol. 7, no. 4, pp. 501-525, October 2002.

21. Russell Tessier, "Fast Placement Approaches for FPGAs", in *ACM Transactions on Design Automation of Electronic Systems*, vol 7, no. 2, pp. 284-305, April 2002.

22. Russell Tessier and Wayne Burleson, "Reconfigurable Computing and Digital Signal Processing: A Survey," in *Journal of VLSI Signal Processing*, Kluwer Publishers, pp. 7-27, May/June 2001.

23. Jonathan Babb, Russell Tessier, Matthew Dahl, Silvina Hanono, David Hoki, and Anant Agarwal, "Logic Emulation with Virtual Wires," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 16., no. 6, pp. 609-626, June 1997.

Conference Publications

1. Jeŕemie Crenne, Patrice Cotret, Guy Gogniat, Russell Tessier, and Jean-Philippe Diguet, "Efficient Key-Dependent Message Authentication in Reconfigurable Hardware", in *Proceedings: IEEE International Conference on Field-Programmable Technology*, New Delhi, India, December 2011.

2. Deepak Unnikrishnan, Justin Lu, Lixin Gao, and Russell Tessier, "ReClick - A Modular Dataplane Design Framework for FPGA-Based Network Virtualization", in *Proceedings: ACM/IEEE Symposium on Architectures for Networking and Communications Systems*, Brooklyn, NY, October 2011.

3. Emmanuel Seguin, Russell Tessier, Eric Knapp, and Robert W. Jackson, "A Dynamically-Reconfigurable Phased Array Radar Processing System", in *Proceedings: 21st International Conference on Field Programmable Logic and Applications*, Chania, Greece, September 2011.

4. Ben Bovée, Mohammad Nekoui, Hossein Pishro-Nik and Russell Tessier, "Evaluation of the Universal Geocast Scheme For VANETs" in *Proceedings: IEEE Vehicular Technology Conference*, San Francisco, CA, September 2011.

5. V. Vijayendra, P. Siqueira, H. Chandrikakutty, A. Krishnamurthy, and R. Tessier, "Real-Time Estimates of Differential Signal Phase for Spaceborne Systems Using FPGAs", in *Proceedings: NASA/ESA Conference on Adaptive Hardware and Systems*, San Diego, CA, pp. 121-128, June 2011.

6. Dong Yin, Deepak Unnikrishnan, Yong Liao, Lixin Gao, and Russell Tessier, "Customizing Virtual Networks with Partial FPGA Reconfiguration", in *Proceedings: ACM SIGCOMM Workshop on Virtualized Infrastructure Systems and Architectures*, New Delhi, India, pp. 57-64, August 2010. **Best Paper Award**

7. Jia Zhao, Basab Datta, Wayne Burleson, and Russell Tessier, "Thermal-aware voltage droop compensation for multi-core architectures", in *Proceedings: ACM Great Lakes Symposium on VLSI*, Providence, RI, pp. 335-340, May 2010.

8. Ramakrishna Vadlamani, Jia Zhao, Wayne Burleson, and Russell Tessier, "Multicore Soft Error Rate Stabilization Using Adaptive Dual Modular Redundancy", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Dresden, Germany, pp. 27-32, March 2010.

9. Deepak Unnikrishnan, Ramakrishna Vadlamani, Yong Liao, Abhishek Dwaraki, Jeremie Crenne, Lixin Gao, and Russell Tessier, "Scalable Network Virtualization Using FPGAs", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, pp. 219-228, February 2010.

10. Tilman Wolf and Russell Tessier, "Design of a Secure Router System for Next-Generation Networks", in *Proceedings: IEEE International Conference on Network and System Security*, Gold Coast, Australia, pp. 52-59, October 2009.

11. Kevin Andryc, Russell Tessier, and Patrick Kelly, "An Interactive Approach to Timing-Accurate PCI-X Simulation", in *Proceedings: IEEE/IFIP International Symposium on Rapid Systems Prototyping*, Paris, France, pp. 181-187, June 2009.

12. Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson and Russell Tessier "A Monitor Interconnect and Support Subsystem for Multicore Processors", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Nice, France, pp. 761-766, April 2009.

13. Deepak Unnikrishnan, Jia Zhao, and Russell Tessier, "Application-Specific Customization and Scalability of Soft Multiprocessors", in *Proceedings: IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa, California, pp. 123-130, April 2009.

14. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, Deepak Unnikrishnan, and Kris Gaj, "Memory Security Management for Reconfigurable Embedded Systems", in *Proceedings: International Conference on Field-Programmable Technology*, Taipai, Taiwan, pp. 153-160, December 2008.

15. David Howland and Russell Tessier, "RTL Dynamic Power Optimization for FPGAs", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Nashville, TN, pp. 714-717, August 2008.

16. Weifeng Xu and Russell Tessier, "Tetris: A New Register Pressure Control Technique for VLIW Processors", in *Proceedings: ACM/SIGPLAN Conference on Languages, Compilers, and Tools for Embedded Systems*, San Diego, CA, pp. 113-122, June 2007.

17. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Eduardo Wanderley, Russell Tessier, and Wayne Burleson, "Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory", in *Proceedings: International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, pp. 146-153, June 2007.

18. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Wayne Burleson, and Russell Tessier, "High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, pp. 117-123, June 2007.

19. Kevin Oo Tinmaung, David Howland, and Russell Tessier, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, pp. 148-155, February 2007.

20. Russell Tessier, Vaughn Betz, David Neto, and Thiagaraja Gopalsamy, "Power-aware RAM Mapping for FPGA Embedded Memory Blocks", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 189-198, February 2006.

21. Lilian Atieno, Jonathan Allen, Dennis Goeckel, and Russell Tessier "An Adaptive Reed-Solomon Errors-and-Erasures Decoder", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 150-158, February 2006.

22. Rishi Khasgiwale, Luko Krnan, Atchuthan Perinkulam, and Russell Tessier "Reconfigurable Data Acquisition System for Weather Radar Applications", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Cincinnati, OH, pp. 822-825, August 2005.

23. Dragana Perkovic, Stephen Frasier, Russell Tessier, Mark Sletten, and Jakov Toporkov, "An Airborne Pod-based Dual Beam Interferometer" in *Proceedings: IEEE Aerospace Conference*, Big Sky, MT, pp. 1193-1201, March 2005.

24. Jian Liang, Russell Tessier, and Dennis Goeckel, "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", in *Proceedings: IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 91-100, April 2004.

25. Andrew Laffely, Jian Liang, Wayne Burleson, and Russell Tessier, "Adaptive System on a Chip: A Backbone for Power-Aware Signal Processing Cores", in *Proceedings: IEEE Conference on Signal Processing*, Barcelona, Spain, pp. 105-108, September 2003.

26. Weifeng Xu, Ramshankar Ramanarayanan, and Russell Tessier, "Adaptive Fault Tolerance for Networked Reconfigurable Systems", in *Proceedings: IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 143-152, April 2003.

27. Jian Liang, Russell Tessier, and Oskar Mencer, "Floating Point Unit Generation and Evaluation for FPGAs", in *Proceedings: IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 185-194, April 2003.

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30. Atul Maheshwari, Russell Tessier, and Wayne Burleson, "Trading Off Reliability and Power Consumption in Ultra-Low Power Systems", in *Proceedings: International Symposium on Quality Electronic Design*, San Jose, California, pp. 361-366, March 2002.

31. Sriram Swaminathan, Russell Tessier, Dennis Goeckel, and Wayne Burleson, "A Dynamically Reconfigurable Adaptive Viterbi Decoder", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 227-236, February 2002.

32. Andrew Laffely, Jian Liang, Prashant Jian, Ning Weng, Wayne Burleson, and Russell Tessier, "Adaptive Systems on a Chip (aSoC) for Low-Power Signal Processing", in *Proceedings: Asilomar Conference on Signals, Systems, and Computers*, Monterey, California, pp. 1217-1222, November 2001.

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34. Ian Harris, Prem Menon, and Russell Tessier, "BIST-Based Delay Path Testing in FPGA Architectures", in *Proceedings: International Test Conference*, Baltimore, Maryland, pp. 364-369, October 2001.

35. Murali Kudlugi, Charles Selvidge, and Russell Tessier, "Static Scheduling of Multiple Asynchronous Domains for Functional Verification", in *Proceedings: 38th Design Automation Conference*, Las Vegas, Nevada, pp. 647-652, June 2001.

36. Murali Kudlugi and Russell Tessier, "Multi-domain Communication for FPGA-based Logic Emulation", in *Proceedings of the 10th International Workshop on Logic and Synthesis*, Lake Tahoe, Nevada, June 2001.

37. Mandeep Singh, Santhosh Thampuran, Prashant Jain, Russell Tessier and Csaba Andras Moritz, "Short Range Wireless Connectivity for Next Generation Architectures" in *Proceedings: International Conference on Parallel and Distributed Processing Techniques and Applications*, Las Vegas, Nevada, June 2001.

38. Wayne Burleson, Russell Tessier, Dennis Goeckel, Sriram Swaminathan, and Prashant Jain, "Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations for Improved Performance and Reduced Power" in *Proceedings: International Conference on Acoustics, Speech, and Signal Processing*, vol. 2, pp. 901-904, Salt Lake City, Utah, May 2001.

39. Ian Harris and Russell Tessier, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures," in *Proceedings: International Conference on Computer Aided Design*, San Jose, California, pp. 49-54, November 2000.

40. Jian Liang, Sriram Swaminathan, and Russell Tessier, "aSOC: A Scalable, Single-Chip Communications Architecture," in *Proceedings: IEEE International Conference on Parallel Architectures and Compilation Techniques*, Philadelphia, Pennsylvania, pp. 37-46, October 2000.

41. Srini Krishnamoorthy, Sriram Swaminathan, and Russell Tessier, "Area-Optimized Technology Mapping for Hybrid FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 181-190, August 2000.

42. Russell Tessier and Heather Giza, "Balancing Logic Utilization and Area Efficiency in FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 535-544, August 2000.

43. Ian Harris and Russell Tessier, "Interconnect Testing in Cluster-Based FPGA Architectures," in *Proceedings: 37th Design Automation Conference*, Los Angeles, California, pp. 472-476, June 2000.

44. Vijay Lakamraju and Russell Tessier, "Tolerating Operational Faults in Cluster-based FPGAs," in *Proceedings: ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, California, pp. 187-194, February 2000.

45. Russell Tessier, "Frontier: A Fast Placement System for FPGAs," in *Proceedings: Tenth IFIP International Conference on VLSI*, Lisbon, Portugal, pp. 125-136, December 1999.

46. Russell Tessier, "Incremental Compilation for Logic Emulation," in *Proceedings: IEEE International Workshop on Rapid System Prototyping*, Clearwater, Florida, pp. 236-241, June 1999.

47. Russell Tessier, "Negotiated A* Routing for FPGAs," in *Proceedings: 5th Canadian Workshop on Field-Programmable Devices*, Montreal, Quebec, pp. 14-19, June 1998.

48. Matthew Dahl, Jonathan Babb, Russell Tessier, Silvina Hanono, David Hoki, and Anant Agarwal, "Emulation of a SPARC Microprocessor with the MIT Virtual Wires Emulation System," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 14-22, April 1994.

49. Russell Tessier, Jonathan Babb, Matthew Dahl, Silvina Hanono, and Anant Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," in *Proceedings: 2nd ACM/SIGDA International Workshop on Field Programmable Gate Arrays,* Berkeley, California, February 1994.

50. Steven Ward, Karim Abdalla, Rajeev Dujari, Michael Fetterman, Frank Honore, Ricardo Jenez, Phillipe Laffont, Ken Mackenzie, Chris Metcalf, Milan Minsky, John Nguyen, John Pezaris, Gill Pratt, and Russell Tessier. "The NuMesh: A Modular, Scalable Communications Substrate", in *Proceedings: International Conference on Supercomputing*, pp. 123-132, July 1993.

51. Jonathan Babb, Russell Tessier, and Anant Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 142-151, April 1993.

Invited Talks

1. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of Arkansas*, Fayetteville, AR, November 2010.

2. "Next-Generation Networking Using FPGAs", Keynote address, *Conference on the Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, July 2010.

3. "Scalable Soft Multiprocessor Generation from a High-level Language", *University of Rennes*, Lannion, France, December 2009.

4. "Scalable Soft Multiprocessor Generation from a High-level Language", *LIRMM*, Montpellier, France, July 2009.

5. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of New Hampshire*, Durham, NH, March 2009.
6. "Hardware Core for Off-chip Memory Security Management in Embedded Sytems", *Boston University*, Boston, MA, November 2008.
7. "Reconfigurable Computing: Research and Curriculum", *University of North Carolina, Charlotte*, Charlotte, NC, May 2008.
8. "Reconfigurable Data Acquisition System for Weather Prediction", *University of Connecticut*, Storrs, CT, February 2008.
9. "Power-Reduction Techniques for FPGAs: Technologies and Trends", *Worcester Polytechnic Institute*, Worcester, MA, December 2007.
10. "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", *Xilinx Corporation*, Edinburgh, UK, July 2007.
11. "Power-reduction Techniques for ReCoSoc: Technologies and Trends", Keynote address, *International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, June 2007.
12. "Reconfigurable Data Acquisition System for Weather Prediction", *Imperial College*, London, UK, June 2007.
13. "A Power-aware BDD Decomposition Algorithm for FPGAs", *University of Toronto*, Toronto, ON, March 2005.
14. "aSoC: A Single-Chip Communications Architecture", *Altera Corporation*, San Jose, CA, February 2004.
15. "aSoC: A Single-Chip Communications Architecture", *University of British Columbia*, Vancouver, British Columbia, August 2003.
16. "Will FPGAs Take Over Systems-on-a-Chip?", *Northeast Workshop on Circuits and Systems panel discussion*, Montreal, Quebec, June 2003.
17. "aSoC: A Single-Chip Communications Architecture", *Carnegie Mellon University*, Pittsburgh, PA., March 2003.
18. "Technology Mapping Algorithms for FPGAs with LUTs and PLAs", *Altera Corporation*, Toronto, Ontario, February 2003.
19. "aSoC: A Single-Chip Communications Architecture", *California Institute of Technology*, Pasadena, CA., January 2003.
20. "A Dynamically-Reconfigurable Adaptive Viterbi Decoder", *Queens University*, Belfast, No. Ireland, August 2002.
21. "Static Scheduling of Multiple Asynchronous Clock Domains for Logic Verification" *Tufts University CAD Seminar,* Somerville, MA., November 2001.
22. "Fast Place and Route Approaches for FPGAs." *Xilinx Corporation,* San Jose, CA, February 1999.
23. "Fast Place and Route Approaches for FPGAs." *University of California, Berkeley CAD Seminar,* Berkeley, CA., February 1999.
24. "Cut-based FPGA Floorplanning for Reconfigurable Computing." *University of Toronto FPGA Research Review,* Peterborough, Ontario, June 1997.