Implementation of 32-Bit Carry Select Adder using Brent-Kung Adder

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Implementation of 32-Bit Carry Select Adder using Brent-Kung Adder

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Abstract
The circuit used to add the two numbers or two bits is adder. The main problem with the adder is both the area and delay to produce the final output. So, this paper implements an adder it requires a less amount of delay and area to produce the final output. The reduction of delay and area is done by the Parallel Prefix Adders. It plays a prominent role in Digital Combinational Circuits. Area and power are other factors which really makes the adder effective. The techniques used to get a less amount of delay and area is by using the Binary-to-Excess-1 Converter (BEC) and a Parallel Prefix Adder. The delay of the Modified Linear Carry Select Adder of Brent Kung Adder is less when compared with the Regular Carry Select Adder architecture. The delay and area further can be improved by using a Square root Carry Select adder. This paper focuses on operation of Parallel Prefix Adders of 32 bit Brent-Kung Adder.

Keywords: And-Or-Inverter (AOI) Logic, Binary-to-Excess-1 Converter (BEC), Brent-Kung (BK) Adders, Carry Select Adder (CSLA), Parallel Prefix Adder

1. Introduction
Design of less consumed area, more accurate and fastest adder logic systems is a very important aspect in the VLSI. In adders propagation of carry signal requires a more amount of time when compared with the final summation output; hence it limits the operation of an adder. One of the important components in the digital circuitry is the adder. It performs an addition operation between two operands by bit-by-bit and generates a carry and sum. The summation and carry output mainly depends upon the delay i.e. no. of transistors present in a circuit, if the circuit occupies a less no of transistors one can easily said that the circuit has less delay and more area efficient. Surprisingly this is one of the important aspects in any digital circuits. In digital circuits each and every component mainly depend upon the power and area, hence most of the circuits are made with less power and more area efficient.

Parallel Prefix Adders are one of the most important techniques to reduce area and delay of the circuit. It can take the help of a Carry Look Ahead adder. Designing of more accurate and high speed adder is called the Carry Select Adder (CSLA).

To solve delay propagation problems, CSLA are used in many digital circuits. It can solve the problem by providing multiple carries and then select the proper carry to produce the final summation. The problem with the CSLA is it is not a less area consumed architecture because presence of multiple Ripple Carry Adder (RCA) for both the carries.

In CSLA architecture the summation and carry outputs are calculated for both $C_{in} = 0$ and $C_{in} = 1$. Depend upon the generated carry the summation output and their respective carry output is selected, and also with the help of a previous carry output the multiplexer (MUX) output is determined by using it as a selection input.
The conventional CSLA contains a two Ripple Carry Adders because of the availability of two RCA's in the circuit the transistor count is increases and due to this the delay also increases, this affects the performance of the circuit badly. Hence, the adder output will be delayed by a more amount of time.

The main aim of this work is to design the architectures which consume less area and delay of an adder, the area can be reduced by interchanging the Ripple Carry Adders one with BK adder and another RCA with BEC add-one mechanism. By using a Square Root architecture (SQRT) the delay will be reduced than the linear architecture because of variable inputs present in each group of SQRT architectures.

The Binary-to-Excess-1 converter (BEC) is one of the add-one schemes. The basic idea behind the BEC is it can add a binary one to the input bits and the output of BEC is given to the multiplexer and another input of the multiplexer is direct input bits. The selection of one of the input bits can be done by the multiplexer (MUX) with the help of a control signals.

In modified regular linear CSLA the Ripple Carry Adder is interchanged with a Binary-to-Excess-1 (BEC) converter because of this the transistor count gradually decreases so; the area occupied by the adder is also reduced. Hence the modified regular linear CSLA gives the final summation and carry outputs within less amount of time. Obviously this is the main aim of any digital circuits.

Organization of this paper is as follows: Section 2 describes the operation of parallel prefix adder. Section 3 explains the area and delay evaluations of basic blocks. Section 4 explains the regular linear CSLA of 32-Bit Brent-Kung (BK) adder and delay evaluations. Section 5 gives the idea about the Modified Regular Linear CSLA of 32-Bit BK adder and delay calculations. Section 6 explains the BK adder simulation results, both Technological and RTL schematics of Brent-Kung Adder and the performance characteristics of the Regular and Modified Linear CSLA of Brent-Kung Adder. The paper is concluded in Section 7.

2. Parallel Prefix Adder

Parallel Prefix Adder used to improve the speed of an addition. These are used to improve the performance of arithmetic circuits in industries due to the improved performance. The design of Parallel Prefix Adder is based upon the three steps:

- Pre-Processing stage.
- Carry Generation stage.
- Post Processing stage.

2.1 Pre-Processing Stage

In this stage generate and propagate signals are calculated for each and every inputs A and B. The signals for this stage are computed by using the equations:

\[ P_i = A_i \oplus B_i \]  
\[ G_i = A_i \land B_i \]  

2.2 Carry Generation Network

At this stage the carries are calculated for every bit and the entire operation at this stage is carried out parallel. At last these generated signals are bisected into smaller pieces. These signals are used as intermediate signals and computed by using the Equations 3 and 4.

\[ CP_{i:j} = P_{i:k+1} \text{ and } P_k \]  
\[ CG_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \]  

2.3 Post Processing Stage

This is the last stage in the Parallel Prefix Adder which is used to calculate the total summation of each and every input bit and it is the final stage for all the adders and these are calculated by using logical Equations 5 and 6.

\[ C_{i-1} = (P_i \land C_{in}) \text{ or } G_i \]  
\[ S_i = P_i \oplus C_{i-1} \]  

3. Area and Delay Evaluation of Basic Blocks

The AND, OR and Inverter (AOI) are the basic building blocks of any logic circuit. The calculation of an area is obtained by simply counting the no. of gates in a circuit. The AND, OR and Inverter occupies a one unit area, while the XOR gate and MUX occupies a 5 and 4 units of delay respectively. The delay methodology considered all gates to be made up of AOI logic and delay for each of the AOI logic is 1 unit. Using this method I can calculate the both area and delay for the CSLA adder blocks these areas and delays are calculated and listed in Table 1.
Table 1. Area and delay evaluations of basic blocks

<table>
<thead>
<tr>
<th>Adder block</th>
<th>Delay</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR Gate</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>2:1 MUX</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>HA</td>
<td>3</td>
<td>6</td>
</tr>
<tr>
<td>FA</td>
<td>6</td>
<td>13</td>
</tr>
</tbody>
</table>

4. Regular Linear Carry Select Adder of 32-Bit Brent-Kung Adder

In parallel prefix adders, its architecture gives a less number of stages to all inputs to outputs with a non-symmetric loading. Parallel prefix adders are one of the unique adders that work on the propagating and generating signals. But the gate level depth of is 0 (log2 (n)), so the speed is lower. The regular linear CSLA of 32-Bit BK adder is shown in Figure 1.

Regular linear CSLA of 32-Bit BK adder has one RCA, BK and a MUX. When compared with the conventional CSLA one RCA is replaced with BK for Cin = 0, hence delay will be reduced. The RCA requires a more no of transistors for the implementation of the adder logic i.e. if the bit size is increases the no. of full adders are increases proportionally. But in the BK adder it requires a less no. of logic gates to implement the same logic, hence the BK adder as less delay and more area efficient. The BK adder follows the tree structure form to increase the speed.

4.1 Delay and Area Evaluation of Regular Linear Carry Select Adder of 32-Bit Brent-Kung Adder

The 32-Bit regular linear CSLA BK adder has 8 groups. Group 1 contains a single BK adder and the remaining groups contains a one BK adder for Cin = 0, a Ripple Carry Adder for Cin = 1 and a Multiplexer. The area and delay evaluation of a 32-Bit Regular linear CSLA BK adder is estimated as follows:

- Group 1 contains a four bit BK adder the delay for the S(0), S(1), S(2), S(3) and final carry c(3) are 3 units, 6 units, 8 units, 10 units and 9 units respectively. Area occupied by these summation and carry outputs are 3 units, 7 units, 9 units, 9 units and 3 units respectively. So, total delay and area occupied in group 1 is 10 units and 31 units.
- Group 2 contains a four bit BK adder the delay and area for them is same as Group 1. The Group 2 also contains a RCA. The four bit RCA as four Full adders and the area and delay occupied by the four bit RCA is 52 units and 12 units. So, total delay and area occupied in Group 2 is 14 units and 114 units.
- Group 3 to Group 8 contains a one BK adder and one RCA hence the area occupied by all these groups are same as Group 2 but the delay will be varied from Group 2 to Group 8 with increasing of 3 units from the previous Groups.

The delay and area evaluation of the 32-Bit regular linear CSLA BK adder is listed in Table 2.

Table 2. Area and delay evaluation

<table>
<thead>
<tr>
<th>Group</th>
<th>Delay</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>31</td>
</tr>
<tr>
<td>2</td>
<td>14</td>
<td>114</td>
</tr>
<tr>
<td>3</td>
<td>17</td>
<td>114</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>114</td>
</tr>
<tr>
<td>5</td>
<td>23</td>
<td>114</td>
</tr>
<tr>
<td>6</td>
<td>26</td>
<td>114</td>
</tr>
<tr>
<td>7</td>
<td>29</td>
<td>114</td>
</tr>
<tr>
<td>8</td>
<td>32</td>
<td>114</td>
</tr>
</tbody>
</table>
5. Modified Linear Carry Select Adder of 32-Bit Brent-Kung Adder

The modified linear CSLA of 32-Bit BK adder is shown in Figure 2. By comparing the modified architecture with the regular CSLA and with the conventional CSLA the modified architecture gives less area because of replacing both the RCA’s as one with the Brent Kung Adder and another with the BEC mechanism. Due to this less area of occupancy the architecture is having a less delay to generate the final summation and carry output.

The modified linear CSLA shows that both the BK adder and a BEC mechanism is connected in a cascade fashion. From Figure 2 the 32-Bit architecture of modified linear CSLA is having eight groups and each group has four input bits to both the Brent Kung and the BEC. The multiplexer is present at the bottom of the architecture and it is used to select one of the summation output depend upon the selection input given to the MUX i.e. the carry of the previous output is used as an selection input to the MUX.

![Figure 2. Modified linear CSLA of 32-Bit Brent-Kung Adder.](image)

5.1 Delay and Area Evaluation of 32-Bit Modified Linear CSLA of Brent-Kung Adder

The 32-Bit modified linear CSLA BK adder has 8 groups. Group 1 contains a single BK adder and the remaining groups contains a single BK adder for $C_{in} = 0$, a BEC for $C_{in} = 1$ and a MUX. The area and delay evaluation of a 32-Bit modified linear CSLA BK adder is estimated as follows:

- Group 1 contains a four bit BK adder the delay for the $S(0)$, $S(1)$, $S(2)$, $S(3)$ and carry output $c(3)$ are 3 units, 6 units, 8 units, 10 units and 9 units respectively. Area occupied by these summation and carry outputs are 3 units, 7 units, 9 units, 9 units and 3 units respectively. So, total delay and area occupied in Group 1 is 10 units and 31 units.
- Group 2 contains a four bit BK adder the delay and area for them is same as Group 1. The Group 2 also contains a RCA. It also contains a four bit BEC and the area and delay occupied by the four bit BEC is 16 units and 6 units. So, total delay and area occupied in Group 2 is 13 units and 90 units.
- Group 3 to Group 8 contains a one BK adder and one BEC hence the area occupied by all these Groups are same as Group 2 but the delay will be varied from Group 2 to Group 8 with increasing of 3 units from the previous Groups.

The delay and area evaluation of the 32-Bit regular linear CSLA BK adder is listed in Table 3.

<table>
<thead>
<tr>
<th>Group</th>
<th>Delay</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>31</td>
</tr>
<tr>
<td>2</td>
<td>13</td>
<td>90</td>
</tr>
<tr>
<td>3</td>
<td>16</td>
<td>90</td>
</tr>
<tr>
<td>4</td>
<td>19</td>
<td>90</td>
</tr>
<tr>
<td>5</td>
<td>22</td>
<td>90</td>
</tr>
<tr>
<td>6</td>
<td>25</td>
<td>90</td>
</tr>
<tr>
<td>7</td>
<td>28</td>
<td>90</td>
</tr>
<tr>
<td>8</td>
<td>31</td>
<td>90</td>
</tr>
</tbody>
</table>

The modified Linear CSLA BK contains a BK adder, BEC fo both $C_{in} = 0$ and $C_{in} = 1$, a MUX. The MUX at the bottom of the architecture will be useful for the summation and carry output. Depend upon the carry of a previous adder the summation of the BK or BEC block will be considered and the previous carry output can be used as a selection input for the multiplexer.
6. Simulation Results

Figures 3 and 4 give the simulation results of a regular and modified Linear CSLA of 32-Bit BK adder respectively.

The inputs for 32-Bit Brent-Kung Adder A and B can be given as “11111111111111111111111111111111” and “11111111111111111111111111111111” the output for this 32-Bit Brent Kung adder’s summation is obtained as a “1111111111111111111111111111111111110” and the output carry is Cout is obtained as “1”. The above mentioned input bit pattern is applicable for both the regular and modified linear carry select adder.

Figures 5 and 6 explain the utilization of both the Regular and Modified Carry Select Adder of 32-Bit Brent-Kung Adder. After performing the simulation synthesis is carried out to see the design utilization of the architectures.

Table 4. Performance parameters of both the regular and modified CSLA of 32-Bit Brent-Kung Adder

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Regular Linear CSLA of BK adder</th>
<th>Modified Linear CSLA of BK adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory (KB)</td>
<td>188684</td>
<td>185228</td>
</tr>
<tr>
<td>Frequency (MHz)</td>
<td>60.998</td>
<td>74.145</td>
</tr>
</tbody>
</table>

From the Table 4 the delay of the Modified Linear Carry Select Adder of Brent-Kung Adder is less when compared with the another architecture because the frequency is more in the Modified CSLA.

Figures 7 and 8 show the technological schematics of a regular and modified Linear CSLA of 32-Bit BK adder.

The technological schematic is obtained only after completing the synthesis process to the targeting phase. It tells about the design by using logic elements in terms of LUTs, carry logic, I/O buffers and other logical components. By viewing this it allows you to see a technology-level representation of HDL optimized for architecture, it will help us to discover design issues early in the design process.
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Figures 9 and 10 give the RTL schematic of regular and modified Linear CSLA of 32-Bit BK adder.

The RTL Schematic tells about the pre-optimized design in the use of symbols such as adders, multipliers, counters, AND gates and OR gates which are totally not depend on the Xilinx devices.

Figure 9. Register transfer level schematic of regular CSLA of 32–bit Brent-Kung Adder.

Figure 10. Register transfer level schematic for modified linear CSLA of 32-Bit Brent-Kung Adder.

7. Conclusion

In this work, a modified regular linear CSLA of 32-Bit BK adder is proposed. When compared with both the conventional CSLA and Regular Linear CSLA BK of 32-Bit adders the proposed model obtains a less amount of delay, speed and area efficient. The further work can be implemented by using a SQRT CSLA and the results will be compared with the regular CSLA. The simulation and synthesis are carried on Xilinx ISE 12.2 on a INTEL core2 (TM).

8. References


