Implementing Design of Modified Area Efficient Enhanced Square Root Carry Select Adder

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Abstract

In the design of Integrated Circuits, area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. In following paper, an area-efficient carry select adder by sharing the common Boolean logic term (CBL) is proposed. Based on this modification a new architecture has been developed and compared with the regular and modified Square-root CSLA (SQRT CSLA) architecture. The modified architecture has been developed using Binary to Excess-1 converter (BEC). The proposed work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in CMOS process technology. The proposed architecture has reduced area, power and delay as compared with the regular SQRT CSLA architecture.

Index Terms: Square Root Carry Select Adder, Ripple carry Adder, Binary To Excess 1 Converter, Common Boolean Logic

1. INTRODUCTION

Design of area and power efficient high speed data logic systems are one of the most substantial areas of research in VLSI system design. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. In electronics applications adders are most widely used. In multipliers, DSP to execute various algorithms like FFT, FIR and IIR. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1. then the final sum and carry are selected by the multiplexers. The basic idea of this work is to use Binary to Excess-1 Converter(BEC) instead of RCA with Cin=1.in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure

2. RELATED WORK

A simple approach is proposed by B. Ramkumar and Harish M Kittur to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes
which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. [1]

HEMIMA.R, CHRISJIN GNANA SUJI.C proposed work uses a simple and efficient transistor level modification to significantly reduce the area and power of the CSLA. Based on this modification 4-bit CSLA architecture have been developed and compared with the regular CSLA architecture. In this proposed architecture RCA was designed using four bit 8T full adder. The multiplexer used in this block was designed with 2T. By reducing the number of transistors used the performance parameters, area and power reduces with slight increase in delay.[2]

Due to importance of adders in signal processing Authorsdesigned a high speed CLA/CSA hybrid adder. Combination of logic styles is an attractive approach for improvement of digital circuits. In this design we used combination of conventional CMOS (C-CMOS) and transmission gate (TG) logic to decrease critical path delay of adder. So with small hardware this adder can operate in very high speed.[3]

Shivani Parmar et.al, Kirat Pal Singh et.al proposed the efficient modified Carry Select Adder (CSA) of 8-bit, 16-bit, 32-bit by using a single Ripple Carry Adder (RCA). The selection of ripple carry adder gives the specifications by accurate resource estimation. The high speed carry select adder performs binary addition pervasive in FPGA applications. Modified carry select adder shows performance and resource improvements as compared with conventional carry select adder. The frequency of conventional CSA is better than modified CSA. This paper proposes a scheme which reduces the delay, area and power than conventional CSA. The overall improvement in Modified CSA shows better results in terms of area power and delay. Hence, proposed modified CSA is being used for power and area efficient devices.[4]

To achieve more speed CSLA is replaces by SQRT CSLA. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [5]-[6]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry input Cin=0 and Cin=1, the final sum and carry are selected by the multiplexers(mux) [7]-[8].

3.PROPOSED WORK

In proposed architecture, an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder is shown in this way, it saves many transistor counts and achieves a low power. Through analyzing the truth table of a single bit full adder, to find out the output of summation signal as carry-in signal is logic ‘0’ is the inverse signal of itself as carry-in signal is logic ‘1’.

By sharing the common Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig. To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the carry signal and summation signal pair. Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal.

Fig: Proposed diagram of 16-bit SQRT CSLA

Fig: Single bit Full adder with CB

This method replaces the BEC add one circuit by Common Boolean Logic. The proposed 16-bit SQRT CSLA architecture is shown in Fig.. The summation and carry signal for full adder which has Cin=1, generate by INV and
OR gate. Through the multiplexer, the correct output result is selected according to the logic state of carry-in signal.

Fig : Individual groups of proposed 16-bit SQRT CSLA

The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly In this paper, an area efficient square-root carry select adder is proposed. By sharing the common Boolean logic (CBL) term, the duplicated adder cells in the conventional carry select adder is removed.

4. Advantages:

From all the reference paper, most recent methods for the carry select adder are discussed. The proposed work is planned to be carried out in the following manner. The reduced number of gates of this work offers the great advantage in the reduction of area. The regular SQRT CSLA has the disadvantage of occupying more chip area. This paper proposes a scheme which reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 32 and 64 bit SQRT CSLA. The reduced number of gates of this work offers the great advantage in the reduction of area.

References:


