Performance Analysis for Full Adder with Zipper Logic

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Abstract—with the shrinking technology, new systems are designed that are miniature in size and perform faster operations. Adder is a basic circuit used for the purpose of addition. In a cascade design, the output of one circuit acts as an input for the other, so delay in the propagation of the carry generated while addition is major issue in the design of adders. When the circuit is designed with any other logic the problem may arise with stored values. During pre-charge, the stored output can affect the circuit. In this paper, we propose Zipper logic for adder circuit so that it prevents any leakage due to stored charge. It also avoids the need of an additional inverter. The proposed adder is designed using cascode circuitry at 45nm with the supply voltage of 1.2V. This improves the speed of operation by replacing inverter with N P block in alternate fashion.

Index Terms—Zipper; NP cmos; charge leakage and charge sharing.

I. INTRODUCTION

With the advancement of technology, new embedded systems are designed with built in power supply and are more power efficient. These systems are capable of performing number of tasks simultaneously such as addition, comparison and multiplications using arithmetic unit. The addition is the most fundamental arithmetic operation in microprocessors as it a basic building block for any mathematical operation. Thus adder design is one of the most significant topics for researcher [1-7]. Besides addition it can perform increment, comparison, multiplication, and division. The adder circuits are very critical to implement in hardware due to the difficulty to predict the evaluation time. Evaluation time mostly depends on carry propagation. In cascade design carry from one full adder propagate to other. As the technology is shrinking, the size of the transistor is reducing and leads to deep submicron effect [8-11]. In an adder circuit the delay variation can occur due to process variations, supply variations, interconnects, environment as well as delay due to carry propagation and which may affect the cycle time. If we find the worst case delay for an adder circuit it is nothing but the product of carry input to carry output and a constant that depends on operand word length and the topology [12-16] for the circuit. As shown in the fig. 1, N bit adder and each full adder has two outputs viz. the sum (S) and carry (C). The carry output for one act as input to other this will add delay due to carry propagation.

In this paper, the performance analysis is done in span of four technologies generation and focused on the evaluation of the delay uncertainty and power analysis. In recent technology zipper logic is one of the most important topology for circuit design. This paper explores the use of the zipper logic for the designing of the full adder circuit. It explain how the zipper logic better than that of other topologies [1]. Delay sensitivity of zipper topologies to supply variations is evaluated analytically, and the results are extensively validated by means of circuit simulations with a 45-nm technology that span four technological generations. The analytical model so derived provides a closer insight to the readers. In any circuit the performance is usually influenced by process fluctuations, supply voltage variations, environmental variations and capacitive coupling between switching nodes. Among the different topologies used for adder circuit design at transistor level, NP CMOS or zipper logic is preferred due to its better performance.

Any circuit is designed using either the static or dynamic technology. The dynamic CMOS logic is transient and can retains the output only for a certain period of time. Dynamic logic can provide temporary storage that last for a certain period of time in contrast with the static logic which stores data for longer duration as power backup is available and hence suitable for high performance applications and in addition it consumes very less power. Static CMOS logic is not much popular as they have timing issues and difficulty in providing clock synchronization. In a dynamic logic the operation performed for a given clock depends on the charging and discharging actions of the capacitive nodes. This process...
has two phases: pre-charge and evaluate. During pre-charge the output is charged to $V_{DD}$ and during evaluate phase output is evaluated. In a dynamic CMOS logic design any of the technologies like pass transistor, transmission gates, domino NP CMOS zipper logic etc. can be used. In this paper, we will discuss some of the dynamic CMOS technologies, their advantages and disadvantages and the implementation method of full adder using zipper logic as it performs better than others.

II. MIRROR FULL ADDER

If we design a circuit using direct static CMOS logic then the number of transistors used is around 28 [17] and results in the increase in the circuit complexity and circuit size. To reduce the number of transistors the same circuit is redesigned using the mirror logic, which reduces the number of transistor to 24 and hence reduces the circuit size, circuit area, the delay introduced by the circuit and finally the load on the carry. In mirror technology, both NMOS and PMOS are used to make pull-up network (PUN) and pull-down network (PDN). In the mirror, they are not dual of each other, rather uses the concept of kill and generate function and is given in table I for one bit full adder. In the given truth table A, B, C are the inputs with two outputs sum(S) and carry(C) and is given by the equations as:

$$SUM(S) = A \oplus B \oplus C$$  \hspace{1cm} (1)

$$CARRY (C) = AB + (A + B)C$$  \hspace{1cm} (2)

Whereas carry output either will propagate or kills gives by the equation as:

$$GENERATE (G) = A.B$$ \hspace{1cm} (3)

$$PROPAGATE (P) = A \oplus B$$ \hspace{1cm} (4)

$$KILL (K) = A.B$$  \hspace{1cm} (5)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>G</th>
<th>P</th>
<th>K</th>
<th>S</th>
<th>C</th>
<th>Carry Status</th>
</tr>
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<tbody>
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<td>0</td>
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<td>0</td>
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<td>0</td>
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<td>0</td>
<td>1</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
<td>Propagate</td>
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<td>0</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Propagate</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Generate</td>
</tr>
</tbody>
</table>

Where as G = Generate, P = Propagate, K = Kill(delete), S = Sum, C = Carry

Another factor in the circuit design is load to carry which is defined as the distribution of the load between the NMOS and PMOS with an assumption that NMOS load resistance is less than that of the PMOS. Hence the ratio for NMOS and PMOS distribution is defined by a constant value k. In fig.2 k is initialized with a value 2. At k=2, the delay due to load will distribute as C$i+6+6+9$ i.e. 11+11=21. The load resistance R is distributed corresponding to the value of k as described in [18]. The most important issue in the circuit is the transistor, which is very close to the load capacitor resulting more capacitance and raises an open issue to reduce it which is a difficult task to deal with.

III. TRANSMISSION LOGIC

The circuits designed using transmission logic employs both of the NMOS and PMOS technologies [19-20]. The CMOS transmission logic is somewhat better than the pass transistor logic because sometimes it becomes difficult to realize the circuit as the output of the pass transistor enters into the undefined state if the gate input goes low. This problem can be solved using transmission logic as the NMOS and PMOS are used in such a way that their gates are controlled through the same supply with an inverter. This topology is based on the concept of propagate and generate model as given in equation (3) and (4). Based on propagated signal, the value for carry input is set either true or complimentary value and gives the output for the sum. In this topology the delay for sum and carry is almost same. If we refer the circuit them we find,

$$SUM(S) = P \oplus C$$ \hspace{1cm} (6)

$$SUM = \begin{cases} C, & \text{when } P = 0 \\ \bar{C}, & \text{when } P = 1 \end{cases}$$ \hspace{1cm} (7)
IV. PASS ADDER

In a pass transistor the circuit is designed with either using NMOS or PMOS [2]. In any circuit conceptually the output is controlled variable and is a function of the input and control signal which are independent variable. The control signal when applied at the gate input, decides which input has to be sent at the output port and which is to be blocked. For NMOS technology, during the charging period the circuit is in source follower mode and will be charged to \((V_{dd} - V_n)\) and during discharge period the circuit discharged to ground. So the maximum peak for charging is \((V_{dd} - V_n)\) which is approx 90% of the maximum voltage [20]. While for a ‘0’ event the NMOS transistor is in common source mode in which the source terminal is at ground and the output discharged to ground. In NMOS pass transistor logic, the discharge time is much less than that of the charge time and this condition gets reversed for its counterpart the PMOS. This time discrepancy sometimes creates problems. Besides this there is another issue related to the power consumption due to leakage and sub-threshold current [21]. In a dynamic logic, leakage current is due to PN junctions present at either the source or drain region of MOS design and hence it is difficult to preserve logic 1. To avoid this problem, bootstrapping is done in which the transistor is charged to a potential higher than that of the peak value. A circuit which has a number of devices connected in series, faces the problem of evaluation phase. When these identical circuit blocks are used in cascade and synchronized with the same clock then there is a race condition during the evaluation. When clock goes high, the logic start to evaluate within finite time and in turn raises the overall delay. This problem can be solved using two clocks instead of one. Domino logic is an example which is using two clocks and hence gives better results.

V. NP CMOS (ZIPPER) ADDER

In zipper logic instead of using N or P both NP block is used and hence it is also named as NP CMOS logic [22-23]. This logic prevents threshold variations and charge sharing problem and provides better stability as compared to the static CMOS logic. In dynamic logic the use of inverter could be overcome by using N and P block connected in alternate fashion. Dynamic topology makes the circuit much faster than static topology. In fig. 5, the zipper logic with NP block is shown with N and P blocks in alternate fashion and so it removes the need of an extra inverter. The circuit is simulated and the results in the form of typical waveforms are shown in fig. 6 with the help of which the behavior of the simulated circuit could be predicted. As the zipper logic uses the N and P evaluation stage in alternate fashion so the pre-charge and evaluation stage are separated from one another and thus prevent any error. The full adder circuit is designed using Cadence Virtuoso using schematic editor at 45nm technology and the simulated design is shown in fig. 7.

VI. PERFORMANCE AND EVALUATION

The transient analysis is done for adder circuit with zipper logic at the supply voltage of 1.2V as shown in fig. 8.
It shows the waveforms of sum and carry output for 3 input bits A, B, and C. The power analysis and delay analysis is done using cadance virtuoso ADL tool. This analysis is done under the variation of supply voltage at the range of 1V to 1.8V and it is concluded that the power increases with respect to supply voltage as shown in fig. 12. The parametric analysis is done under the channel width variation with the step range of 1μm to 10μm which shows power varies as a function of channel width.

Transient power and DC power analysis is done which is shown in fig. 9 and fig. 10 respectively. In the DC power analysis power increases with the supply voltage. The circuit design with NP CMOS (zipper) logic gives better result as the power varies in the range of 0.1μW to 1μW which is very less. With the help of the results shown in fig. 12 it can be concluded that power dissipation in the zipper logic is much less than that of the mirror logic.
Similarly the delay analysis is also done with the supply voltage variations in the range of 1V to 1.8 V. The delay analysis is to find the time taken by the logic circuit to give the response. Through fig. 13 it is noticed that the delay for zipper logic varies in the range of 0.016ns to 0.121ns which is very less compared to other logics. So we can conclude that the delay reduced with increase in supply voltage.

### TABLE II. POWER ANALYSIS DATA

<table>
<thead>
<tr>
<th>Vdd</th>
<th>Zipper Logic (uW)</th>
<th>CPL Logic (uW)</th>
<th>Mirror Logic (uW)</th>
<th>Transmission Logic (uW)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
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<td>0.01652</td>
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<td>0.0813</td>
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<tr>
<td>1.8</td>
<td>1.09</td>
<td>0.139</td>
<td>1.782</td>
<td>0.526</td>
</tr>
</tbody>
</table>

Fig. 12. Power analysis with supply voltage variation

### TABLE III. DELAY ANALYSIS DATA

<table>
<thead>
<tr>
<th>Vdd (V)</th>
<th>Zipper Logic (ns)</th>
<th>CPL Logic (ns)</th>
<th>Mirror Logic (ns)</th>
<th>Transmission Logic (ns)</th>
</tr>
</thead>
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</tbody>
</table>

Fig. 13. Delay analysis versus supply voltage variation

### VII. CONCLUSION

In this paper we have designed analytical model of full adder with different topologies and performance analysis is done. Through power and delay analysis we have concluded that the zipper logic gives better result. With the experimental result it was shown that the power is increases with supply voltage $V_{dd}$. This technology is robust against threshold voltage violation. The speed of operation is improved and prevent from charge sharing and charge leakage problem. The analysis is done at room temperature 27°C and it is found that at 1.2V the power dissipation was 0.196µW and delay was 0.02ns. The speed performance is achieved with the supply voltage variation. In the design NMOS and PMOS block are used separately in alternate fashion and so overcome the need of inverter. Although the other topologies as CPL and transmission logic roughly gives the same result but better than mirror logic. As far considered the effect of dimensional scaling by the parametric analysis we have found that the power varies with channel width.

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