Performance Analysis of Dual Gate MOSFET Arithmetic Logic Unit

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Abstract - This paper presents Dual Gate MOSFET (DGMOSFET) for digital application. The digital application discussed here for DGMOSFET is ALU (Arithmetic Logic Unit). A 1-bit ALU has been designed and simulated, which implements four basic operations like NAND, NOR, XOR, and Addition. The Simulation of ALU is carried at 32nm, 45nm and 65nm MOS Process technologies. The results obtained from simulation of DG ALU are compared with conventional MOS ALU. The figures of merit measured for ALU are power and delay. At 32nm and 45nm technology, power in DGMOSFET was found out to be 20.3% and 24% respectively less than the MOS ALU at same technology. The delay of ALU was found to be 26.36% less than MOS ALU at 32nm and 16.32% less at 45nm technology. All the results are carried out using Tanner EDA tools.

Keywords- DGMOSFET, ALU, power, delay, simulation.

I. INTRODUCTION

The Integrated Chip (IC) Technology has revolutionized the world of electronics in which MOS transistors have played a vital role in enhancing performance of integrated devices. In order to achieve high circuit density and performance, MOS chips are continuously being scaled from last two decades. This has lead to enhanced performance, reduced Cost per Gate in today’s system. According to ITRS, MOSFET with 16nm gate length will be available in 2010, of 10nm in 2015, 6nm in 2020 [1]. But there is certain limitation up to which this gate length can aggressively be scaled. So, the need arises to look for alternative device structures such as Dual Gate MOSFET (DGMOSFET) which is proposed for sub nano regimes. As the name suggests, DGMOSFET has two gates, which adds into flexibility of the device. A lot of research has been done in the field of DGMOSFET structure and its physics, but much work has to be done at DG circuit level. There are numerous applications of DGMOSFET in digital and in analog field such as reconfigurable gates which can perform multiple operations, variable gain amplifiers, high frequency mixers etc.

ALU is the fundamental unit of processor in a computer. ALU performs various logical and arithmetic functions. ALUs also contribute to one of the highest power-density locations on the processor, resulting in thermal hotspots and sharp temperature gradients within the execution core [2]. Hence it becomes extremely important to control the power of an ALU. The delay and power of ALU are directly proportional to each other, so a tradeoff has to be maintained between two of them.

II. DUAL GATE (DG) MOSFET

Scaling is simply referred to as diminution in the device dimensions. This scalability of a device is increased by introducing a second gate at the other side of the body of each transistor leading to a dual-gate SOI structure (Figure 1). Because of presence of two gates, excellent control of the short channel effects is achieved, since the capacitance gets double with the presence of two gates due to which the voltage of the channel is controlled efficiently. Dual-gate SOI devices have emerged as the device of choice for circuit design below sub-50 nm regime [3]. Low sub threshold leakage current and higher ON-current in the dual -gate devices make them suitable for circuit design in sub-50 nm regime [4, 5]. There are three most commonly used structures of dual gate MOSFET i.e. planar, vertical and FinFET, out of which one of the promising structures in the dual-gate technology is FinFET [6] owing to its simple fabrication process (Figure 2). ITRS reports also show the inevitable inclusion of DGMOSFETs in many upcoming VLSI applications [7]. DGMOSFETs for optimal sub-threshold operations have also been considered recently [8–14]. DGMOSFETs are suitable for the sub-threshold operation due to their near ideal sub-threshold slope and negligible junction capacitance. DGMOSFETs have the following advantages over bulk CMOS technology [15]:

1. Reduction in device area.
2. The miller capacitance and output conductance are further reduced, making the dual gate MOSFET a useful device for analog integrated circuits.
3. The reduced feedback and the resulting increase in power gain and stability, in conjunction with the increased functional capabilities stemming from the presence of two independent control gates.
4. The break down voltage can be made very high with proper design.
5. The short channel effects are considerably diminished.
7. Smaller junction capacitances.
8. Better immunity to SCEs, although negligible for sub-threshold operation.
10. Design flexibility at circuit level by symmetric/asymmetric with tied and independent gate options. In tied gate configuration both the gates i.e. front and the back gate are tied together and are biased with the same source while in independent gate configuration both the gates are independently biased.

The electrostatics of the DGMOSFET can be divided into two broad categories as symmetrical and asymmetrical. The symmetric devices have the same gate bias and work function and hence turn ON at the same time. The asymmetric devices can have different bias and work functions.

**A. Design of DGMOSFET**

Two single transistors connected together can be considered to be equivalent to DGMOSFET. The transistors are connected in parallel forming electrical connections at the source and the drain region. Each transistor has its own parameters such as threshold voltage and oxide thickness. The length and width of the each single transistors used is kept same. The drain current for two parallel transistors in linear region is given by

\[ I = \frac{W}{L} \left[ \mu_1 C_{ox1}(V_{g1} - V_{t1}) + \mu_2 C_{ox2}(KV_{g2} - V_{t2}) \right] \]

III. ALU DESIGN

The top-level module consists of a single bit ALU. A general eight function instruction set for CMOS ALU performs the following: addition, subtraction, AND, NAND, OR, NOR, XOR and XNOR. Each of these functions is performed on two one-bit input bitwise operations. The bitwise output results go to the 8:1 multiplexer, where multiplexer selects one of the results to the output. Each of the single bit building blocks are cascaded together to form a four bit ALU. Figure 3.1 shows general block diagram of an 1-bit ALU. Such kind of architecture results in simultaneous execution of all the functions.

**A. CMOS Design Methodology**

In CMOS Design methodology the main part of ALU design is adder. To implement ALU we use 4:1 MUX, NAND Gate, NOR Gate, XOR Gate and a modified adder.

1) Adder

Adders are implemented in different ways serving different Speed or Density requirements. Conventional CMOS Full Adder is given by the equation

\[ \text{Sum} = (A \text{xor } B) \text{xor } C \]
\[ \text{Carry} = AB + AC + BC \]

Usually in full adder A and B are adder inputs, C is carry. The logic is implemented by using n-channel and p-channel transistors in case of conventional CMOS full adder. So the total number of transistors used here is double. The total number of transistors used in fig. 3.1.1 is 40. Increased number of transistors used results in delay and increase in area. The fig.3.1.2 is schematic of modified full adder.
2) **4:1 MUX**

Fig. 3.1.4 shows 4:1 multiplexer (MUX) formed by using three 2:1 multiplexer available in Tanner S-Edit library. The function of multiplexer is to select one of many inputs which are selected by setting the select signal s0 and s1.

3) **NAND Gate**

Inst Two input NAND gate is shown in fig. 3.1.4 where A and B are inputs while AB is the output. To implement this NAND gate function, PMOS transistors are connected in parallel while the NMOS transistors are connected in series.

4) **NOR Gate**

Two input NOR gate is shown in fig. 3.1.5 where A and B are inputs while out2 is the output. To implement this NOR gate function, PMOS transistors are connected in series while the NMOS transistors are connected in parallel.

5) **XOR Gate**

Fig. 3.1.6 shows XOR gate with two inputs A and B, while y is the output. XOR Gate is implemented using one AOI12 and one NOR gate. So, in this schematic XOR gate is implemented without inverters.
6) **CMOS ALU Design**

ALU is implemented in fig. 3.1.7 with all the functionality blocks implemented separately are combined in one. The benefit of this design is that, all computations are performed parallel so no clock resources are wasted. The waveforms are shown in fig. 3.1.8. When \( A= 0, B= 0, C=1 \) then sum = 0 and carry is 1.

![Fig. 3.1.7 Schematic of ALU](image)

![Fig. 3.1.8 Simulation of CMOS ALU performing addition](image)

**B. Dual Gate Design Methodology**

The design methodology for designing of Dual Gate ALU is similar to that of MOS ALU. All sub modules are designed using N type DGMOSFET and P type DGMOSFET. The symbol of N channel DGMOSFET is shown in fig.3.2.1.

![Fig. 3.2.1 Symbol of N channel DGMOSFET](image)

1) **DG NOR Gate**

Two input NOR gate is shown in fig. 3.2.4 where A and B are inputs while out2 is the output. To implement this NOR gate function, DG PMOS transistors are connected in series while the DG NMOS transistor is connected in parallel.

![Fig. 3.2.2 Schematic of DG NOR gate](image)

![Fig. 3.2.3 Schematic of DG NAND gate](image)

2) **DG NAND Gate**

Two input NAND gate is shown in fig. 3.2.6 where A and B are inputs while \( AB \) is the output. To implement this NAND gate function, DG PMOS transistor is connected in parallel while the NMOS transistors are connected in series.

![Fig. 3.2.4 Schematic of DG XOR gate](image)

3) **DG XOR Gate**

Figure 3.2.8 shows XOR gate with two inputs A and B, while y is the output. XOR gate is implemented using one DG AOI123 and one DG NOR gate. So, in this schematic XOR gate is implemented without inverters.

4) **DG Full adder**

The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. In Fig. 3.2.5.
5) **DG ALU**

DG ALU is implemented and the waveforms are shown in fig. 3.2.7 for inputs \(A=0\) \(V\), \(B=0\) \(V\) and \(C=0\) \(V\). The select signal value is “00” hence NAND operation is performed on the input signal and the output is 1.

### IV. SIMULATION RESULTS

Each of the DG ALU functions are performed on a single bit input in Tanner S-edit using 32nm, 45nm, 65nm technology. Performance analyses are performed using Tanner Spice. The design has been simulated using 32nm, 45nm, 65nm process technology as shown in Table 4.1. The large propagation delay or critical path within the circuit and improving the hardware which causes delay is a standard method for increasing the performance. The maximum critical path delay is 8.98ns at 65nm technology and minimum critical path delay is 8.1ns at 32nm technology of DG ALU. If the delay comparison results with the conventional ALU and DG ALU, the maximum delay is 11ns in conventional ALU and 8.1ns in DG ALU at 32nm process technology. The power consumption of DG ALU is much better than conventional ALU. The graphical representation of power consumption and delay are shown in Fig. 4.1 and Fig. 4.2. The performance comparison result at different technologies shows that in DG ALU the power was reduced by 20.3% while the delay was found to be 26.36% less than conventional ALU.

<table>
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<tr>
<th>Module</th>
<th>parameters</th>
<th>32nm Technology</th>
<th>45nm Technology</th>
<th>65nm Technology</th>
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<tr>
<td>ALU</td>
<td>Power((uW))</td>
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<td>2.5</td>
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<tr>
<td></td>
<td>Delay((ns))</td>
<td>11</td>
<td>9.8</td>
<td>11</td>
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<tr>
<td>DG ALU</td>
<td>Power((uW))</td>
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<td>1.9</td>
<td>2.8</td>
</tr>
<tr>
<td></td>
<td>Delay((ns))</td>
<td>8.1</td>
<td>8.2</td>
<td>8.98</td>
</tr>
</tbody>
</table>

![Fig. 4.1 Power consumption in ALU and DG ALU](image1)

![Fig. 4.2 Delay in ALU and DG ALU](image2)
V. CONCLUSION

The DG ALU implemented is a single bit ALU with only four basic operations implemented in it. The same ALU can be cascaded to form 4 bit or higher order ALU. The number of functions implemented can also be increased from four by incorporating more logical and arithmetic operations such as rotate, multiplication, subtraction, carry overflow and many more operations.

VI. FUTURE SCOPE

The DG ALU implemented was used DG MOSFET adder, NOR Gate, NAND Gate, and XOR Gate which resulted in lesser delay and power consumption within the circuit. While implementing different gates in different technologies it was seen that DGMOSFET consumes less power than conventional MOSFET. The results carried out in 32nm process technology gives better results than the circuits implemented in 45nm or 65nm technologies.

VII. REFERENCES