Hyeran Jeon

e-mail: hyeran.jeon@sjsu.edu

Office: TBD

Tel: (213)359-3829

Assistant Professor, San Jose State University, San Jose, CA

Faculty member, Dept. of Computer Engineering, College of Engineering (Aug. 2015~)

Research areas: Computer architecture, energy efficient and reliable computer design, throughput processor design, emerging memory system design and embedded and cyber-physical system

EDUCATION

PhD in Computer Engineering ····· Aug. 2009 – Aug. 2015

University of Southern California, Los Angeles, CA

Advisor: Dr. Murali Annavaram

Thesis: Resource Underutilization Exploitation for Power Efficient and Reliable Throughput Processor

MS in Computer Science ····· Jan. 2007 – May. 2008

Georgia Institute of Technology, GA, US and

Korea University, Seoul, Korea (Dual Degree program)

Thesis Advisor: Dr. Sung Woo Chung

Thesis: Load Unbalancing Strategy for Multi-Core Embedded Processors **[J1]**

BS in Computer Engineering ····· Mar. 1997 – Feb. 2002

Pusan National University, Pusan, Korea

RESEARCH EXPERIENCE

University of Southern California, Los Angeles, CA ····· Aug. 2009 – Aug. 2015

Research Assistant

- **Energy efficient, Reliable, and High-performance Many-core Architecture Design**

  Memory prefetching algorithm design for GPGPU **[T1, C1]**

  Proposed a novel prefetching algorithm for GPGPU that exploits the regularity and irregularity detected in the memory accesses of different thread groups, and implemented and evaluated the idea on GPGPU-Sim simulator

  Energy efficient GPGPU register file design **[T2, C2, C3]**

  Proposed a novel GPU register management method that can save both static power and dynamic power of GPU register file by incorporating a simple power gating and register file under-provisioning, and implemented and evaluated the idea on GPGPU-Sim simulator

  Architectural support for reliable GPGPU computing **[C4, C5]**

  Proposed a novel error detection method for GPGPU execution units that exploits the underutilized resources for computation verification, and implemented and evaluated the proposed idea on GPGPU-Sim simulator

- **Workload Characterization**

  Detailed memory sub-system performance characterization for GPGPU **[C6]**

  Detailed micro-architectural characterization of graph applications on GPGPU **[C7]**

Coordinated the experiment to get the graph application characteristics, ran the graph applications on the real GPU and analyzed the results

- **Application Parallelization on CPU-GPGPU Heterogeneous system**

  Junction tree scheduling methods of exact inference **[C10, C11]**

  Proposed an efficient scheduling algorithm for parallelizing the exact inference on GPGPU and implemented and evaluated the proposed idea by using CUDA-C

AMD Research, Bellevue, WA ····· Sep 2012 – Dec 2012

Research Coop

- **GPGPU AVF Modeling [W1]**

  Integrated AVF model to AMD's heterogeneous computing platform simulator and analyzed the AVF of register file and instruction buffer of GPU while running rodinia and CUDA-SDK benchmarks

- **Reliable Memory System Design [C8, P1]**

  Proposed a novel error detection and correction code for die-stacked DRAM and implemented and evaluated the proposed idea on Macsim simulator

IBM T.J. Watson Research Center, Yorktown, NY ····· May 2012 – Aug 2012

Summer Research Intern

- **Efficient and Reliable FTL Design for Flash based SSD [C9]**

  Integrated Hadoop platform to AIX operating system, implemented several hybrid FTL management algorithms to the SSD simulator, ran Hadoop applications on the SSD simulator and analyzed the behaviors of the Hadoop workloads

TEACHING EXPERIENCE

University of Southern California, Los Angeles, CA

- TA for EE101 Introduction to Digital Logic ····· Fall 2010, Fall 2011
- TA for EE352 Computer Organization and Architecture ····· Spring 2011, Summer 2011, Spring 2012
- TA/Guest Lecturer for EE557 Computer Systems Architecture ····· Spring 2014
- Guest Lecturer for EE352 Computer Organization and Architecture ····· Spring 2011
- Guest Lecturer for EE653 Advanced Topics in Microarchitecture ····· Spring 2012
- Guest Lecturer for EE598 Electrical Engineering Research Seminar ····· Fall 2012, Spring 2013

INDUSTRY EXPERIENCE

Samsung Electronics, Co., LTD. Kiheung, Korea ····· Feb. 2002 – Apr. 2009

Department: SOC research center, System LSI Division

Job Title: Systems Software Engineer

- **RTOS integration to channel platform**

  Developed hardware abstraction layer (HAL) for ARM7TDMI and board support package (BSP) for channel platform

- **Multi-core RTOS development**

  Managed the project and developed several kernel modules (synchronization, inter-core communication, load balancing, and per-core data utilization), HAL for ARM11 MPCore, and BSP for PB11MPCore and CT-EB11MPCore board **[P2]**

- **Linux integration to ADSL modem**

Developed several device drivers (uBoot, PCI host Controller and DMA controller) and a web based modem configuration program

- **TPM software stack development**
  Designed and developed a software stack (TSS service provider) for trusted platform module (TPM) **[C12, P3]**

HONORS AND AWARDS

- *Viterbi Dean's Doctoral Fellowship* from University of Southern California, US ····· 2009-2013
- *Nominated as a top graduate student in EE department of the year* by USC WiSE Merit award·····2014
- *Nominated for Intel PhD Fellowship* by University of Southern California, US ·····2014
- *Student Travel Grant Awards* by MICRO'12, Grad Cohort Workshop'12, CRA-W/CDC Computer Architecture Summer School'12, and IISWC'14·····
- *Scholarship for graduate study* from Ministry of Information and Communication, Korea ····· 2007-2008
- *Scholarship for graduate study* from Samsung Electronics, Korea ····· 2007-2008
- *Scholarship for outstanding student* from LG Electronics, Korea ····· 2001-2001
- *Scholarships for academic achievement* from Pusan National University, Korea ····· 1997-1999

PUBLICATIONS

Journal Papers

Energy Efficient Scheduling Algorithm for Multi-Core Mobile Processors

J1. **Hyeran Jeon**, Woo Hyong Lee, Sung Woo Chung, "Load Unbalancing Strategy for Multi-Core Embedded Processors", IEEE Transactions on Computers (TC), vol. 59, no. 10, pp. 1434-1440, October 2010

Conference/Workshop Papers

Energy efficient, Reliable, and High-performance Many-core Architecture Design

C1. **Hyeran Jeon**, Gunjae Koo and Murali Annavaram, "CTA-aware Prefetching for GPGPU", *under review*

C2. **Hyeran Jeon** and Murali Annavaram, "GPGPU Register File Virtualization", *under review*

C3. Sangpil Lee, Keunsoo Kim, Gunjae Koo, **Hyeran Jeon**, Won Woo Ro, and Murali Annavaram, "Register File Compression for Power Efficient GPGPU", The 42th International Symposium on Computer Architecture (ISCA), Portland, OR, Jun 2015

C4. Mohammad Abdel-Majeed, Waleed Dweik, **Hyeran Jeon**, and Murali Annavaram, "Low-Cost Fault Detection and Correction in GPGPUs", IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Rio De Janeiro, Brazil, Jun 2015

W1. **Hyeran Jeon**, Mark Wilkening, Vilas Sridharan, Sudhanva Gurumurthi and Gabriel Loh, "Architectural Vulnerability Modeling and Analysis of Integrated Graphics Processors", IEEE Workshop on Silicon Errors in Logic - System Effect (SELSE), Stanford, CA, March 2013

C5. **Hyeran Jeon** and Murali Annavaram, "Warped-DMR: Light-weight Error Detection for GPGPU", The 45th IEEE/ACM International Symposium on Microarchitecture (MICRO), Vancouber, BC, Dec 2012

Workload Characterization

C6. Gunjae Koo, **Hyeran Jeon** and Murali Annavaram, "Revealing Critical Loads and Hidden Data Locality in GPGPU applications", to appear in IEEE International Symposium on Workload Characterization (IISWC), Atlanta, GA, Oct 2015

C7. Qiumin Xu, **Hyeran Jeon** and Murali Annavaram, "Graph processing on GPUs: Where are the bottlenecks?", IEEE International Symposium on Workload Characterization (IISWC), Raleigh, NC, Oct 2014

Reliable Memory System Design

C8. **Hyeran Jeon**, Gabriel H. Loh and Murali Annavaram, "Efficient RAS support for Die-stacked DRAM", IEEE International Test Conference (ITC), Seattle, WA, Oct 2014

Efficient and Reliable FTL Design for Flash based SSD

C9. **Hyeran Jeon**, Kaoutar El Maghraoui and Gokul Kandiraju, "Investigating Hybrid SSD FTL Schemes for Hadoop Workloads", ACM International Conference on Computing Frontiers (CF), Ischia, Italy, May 2013

Application Parallelization on CPU-GPGPU Heterogeneous system

C10. **Hyeran Jeon**, Yinglong Xia and Viktor K. Prasanna, "Parallel Exact Inference on a CPU-GPGPU Heterogeneous System", The 39th International Conference on Parallel Processing (ICPP), San Diego, CA, Sep 2010

C11. **Hyeran Jeon**, Yinglong Xia, Viktor Prasanna, "Node Level Primitives for Exact Inference on GPGPU", The 17th International Conference on Systems, Signals and Image Processing (IWSSIP), Rio de Janeiro, Brazil, Jun 2010

Software Modeling for TPM Software Stack

C12. Jongil Park, Jisung Kim, **Hyeran Jeon**, Kyungmin Cho, "The Modeling of TPM Software Stack based on Software Development Process and UML", Samsung Technology Conference, Kiheung, Korea, 2005

Technical Reports

T1. **Hyeran Jeon**, Gunjae Koo and Murali Annavaram, "CTA-aware Prefetching for GPGPU", Technical Report (CENG-2014-08), Department of Computer Engineering, University of Southern California, Oct 2014

T2. **Hyeran Jeon** and Murali Annavaram, "Energy Efficient GPGPU Register File Design Through Lifetime Aware Register Renaming", Technical Report (CENG-2014-05), Department of Computer Engineering, University of Southern California, May 2014

Patents

P1. **Hyeran Jeon** and Gabriel H. Loh, "Performing logical operations in a memory" (US20150199150 A1)

P2. **Hyeran Jeon**, Woohyong Lee, Mingyu Lee, Woongee Kim, Jiseong Oh, Jagun Kwon, and Taekgyun Ko, "Multi-processor system device and method declaring and using variables" (US 20100250851)

P3. Jongil Park, Jisung Kim, **Hyeran Jeon**, Kyungmin Cho, "TSS Persistent Storage management method by using file system" (KP 10-2006-0044398)

STUDENT MENTORING

- Ranjan Anantharaman (Undergrad at BITS-Pilani and visiting scholar for Viterbi-India program)
  Assigned and guided a project, GPGPU Architecture Optimization for Irregular Workload Execution, and helped the poster presentation

PROFESSIONAL ACTIVITIES

Invited Reviewer

- IEEE Design & Test ····· 2015
- IEEE Micro ····· 2015
- IEEE International Symposium on High Performance Computer Architecture ····· 2015
- IEEE/ACM International Symposium on Microarchitecture ····· 2014
- ACM Transactions on Design Automation of Electronic Systems ····· 2013, 2014
- Workshop on Parallel and Distributed Computing for Machine Learning and Inference Problems ····· 2012
- IEEE Transactions of Parallel and Distributed Systems ····· 2011
- IEEE International Symposium on Field-Programmable Custom Computing Machines····· 2011

Invited Speaker

- Poster presentation at DARPA PERFECT PI meeting ····· 2014

Student Volunteer

- IEEE International Parallel & Distributed Processing Symposium ····· 2010