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Performance and Mitigation Strategy of Distributed AC-Stacked PV Inverter Architecture under Grid Background Harmonics

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Abstract—Grid-tied Photovoltaic (PV) inverters are required to have harmonics mitigation control to reduce harmonics distortion on the output current caused by the impact of grid background harmonics. In this paper, a decentralized control strategy for reduction of the impact of distorted grid voltage on the AC-stacked PV inverter architecture is proposed. Two control schemes with the selective harmonics mitigation strategy and without any handshaking among the inverters are proposed for this architecture and analyzed to present the improvement of the power quality as well as the operating margin of the architecture. The proposed methods are analyzed by impedance analysis and verified their feasibility and performance through a controller hardware-in-the-loop test.

Index Terms—AC-stacked PV inverter, decentralized harmonics mitigation control, grid background harmonics, modular PV inverter control, operating margin analysis.

I. INTRODUCTION

Participation of Photovoltaic (PV) power generation in electric power grid has increased considerably due to growing energy demand and environmental issues. The electrical grid is responsible for providing regulated power at a high-quality standard to the load with the presence of high penetration of intermittent PV generations. This requires the grid to have load following functions such as voltage and frequency regulation, and the supply of reactive power and harmonic currents [1]–[4]. Some load following functions can be achieved by appropriate control of the PV inverters as well [5]–[7].

The impact of renewable energy sources on grid voltage background harmonics, especially in networks with high penetration of distributed generations, has been presented in [8]–[11]. On the other hand, in grid-connected inverters, the harmonic profile of the inverters output current can be affected by the variations in the grid voltage background harmonics [12]–[15]. To provide high-quality power to the grid, a robust background harmonic mitigation control method for the grid-connected inverters is required [16]–[18].

One of the main reasons of output current distortion in a grid-connected inverter under grid background harmonics is that the low output impedance of the inverter provides a path for the grid harmonics. To mitigate the negative impact of grid voltage background harmonics and improve power quality using renewable energy sources, particularly PV inverters, it is required to have proper control strategy to increase the output impedance of the inverter for grid harmonics. A Proportional-Resonant (PR) controller is appropriate to mitigate the impact of the grid background harmonics. It introduces an infinite gain at a selected resonance frequency for eliminating steady-state error [19].

This paper investigates two control strategies suppressing the impact of grid background harmonics and proposes an effective strategy for the grid-tied AC-stacked PV inverter architecture. The AC-stacked PV inverter topology is the new panel-level architecture, which provides high-efficiency and lower-cost by stacking high-frequency and low-voltage modular inverters in series. This architecture and its tangible advantages were introduced in [20], [21]. This architecture utilizes AC voltage optimization per-phase and per-string [22], [23]. Power optimization is performed at both the individual panel level and the AC string system level. To maximize the effectiveness of the proposed architecture, each building block is controlled independently with no communication among themselves and minimum handshaking synchronization information with supervisory control [21].

In one method, a single inverter compensates for the background harmonics by utilizing additional PR controllers, and in the second method, all the inverters are participating in the harmonics mitigation. Feasibility and performance of these control methods have been analyzed and verified by numerical analysis and Controller Hardware-In-the-Loop (CHIL) test.

The rest of the paper is organized and presented as follow. Section II presents the AC-stacked PV inverter architecture. Details of proposed harmonic mitigation control scheme and impedance analysis are introduced in Section III. Section IV provides the results and discussion followed by Section V as conclusion.
II. AC-STACKED PV INVERTER ARCHITECTURE

The AC-stacked PV inverter architecture, a distributed cascaded inverter topology suitable for grid-tied PV applications, as shown in Fig. 1. In this architecture, multiple module-level PV inverters are connected in series and cooperate to maintain AC string output voltage for the grid-connection. Also, they perform Maximum Power Point Tracking (MPPT) control with their individual PV panels. This panel-level configuration has the advantage of utilizing low-voltage high-frequency semiconductor devices such as MOSFETs. Also, this configuration has a fully decentralized operation environment.

A decentralized control scheme was proposed for this architecture in [21], [23], [25]. In this control scheme, a Current Administrator Voltage Compensator (CAVC) not only controls its DC input voltage for MPPT control of PV panel but also is responsible for controlling the AC string current, and Voltage Mode Members (VMM) control DC input voltages for MPPT control of individual PV panels and build up output voltage. Proportional-Integral (PI) controller is applied to control individual DC input voltages of each inverter member, and PR controller is applied to control the fundamental frequency content (60Hz) of the AC string current in CAVC. Based on the decentralized control scheme, each inverter is controlled autonomously by using its local measurements. The different capability of this architecture such as active and reactive power control, and smart inverter functionalities are studied in [16], [21], [25], [26]. In the next section, a modified control scheme is proposed to mitigate the impact of the grid background harmonics and improve the power quality of the AC-stacked inverter system.

III. GRID BACKGROUND HARMONICS MITIGATION CONTROL SCHEME

To study the impact of grid background harmonics on the output current and the mitigation technique, we need the modeling of the current control loop of this system.

A. Single-member harmonics compensation

It can be assumed that input DC voltage ripple is negligible if DC-bus capacitors are large enough in the circuit presented in Fig. 1. Also, DC voltages are considered as constant since DC voltage control loops are much slower than current control loop. PWM generators can be modeled as the proportional gain ($K_{PWM}$) using average switching model if the switching frequency is high enough.

The first harmonics compensation method proposed for this architecture is Single-member Harmonics Compensation (SmHC), where only CAVC participates the compensation. In this manner, additional PR controllers are applied for selective harmonics, and the reference for these controllers is zero and the output of these controllers are added to the modulation index with the output of the PR controller for the fundamental harmonics. The block diagram of this method is presented in Fig. 2 where $I_r$ is the reference current, $G_C$ is a PR compensator for fundamental frequency, $G_{PR5th}$ and $G_{PR7th}$ are PR compensators for grid background harmonics, $M_n$ is modulation index of each inverter, $V_{Cn}$ is the capacitor voltage of each inverter, and $I_g$ is the AC string output current.

In the closed-loop current control model in Fig. 2 the same passive components, $L_n$ and $C_n$, are considered in three individual inverters, and a current controller with the PR compensators and the current feedback term are considered in CAVC only. VMMs only build up the voltage based on their modulation indices for grid-connection. In SmHC, closed-loop control blocks, $G_{PR5th}$ and $G_{PR7th}$, are added in CAVC for the compensation of 5th and 7th background harmonics.

Bode plot of impedance of individual inverter voltage disturbance to the AC string current in the SmHC are presented in Fig. 3. As the system parameters, 45V\text{RMS} electrical grid, three PV inverters, and inverter components parameters are considered as presented in Fig. 1. For grid-connection with

Fig. 1: AC-stacked grid-tied PV inverter system consisting three inverters in a string

Fig. 2: Block diagram of SmHC for AC-stacked PV inverter system.
conventional 120V_{RMS} electrical grid, this architecture can be extended to eight PV inverters. The PR controller provides the high impedance at the selected frequency. Therefore, the grid background harmonics, 5^{th} and 7^{th}, cannot impact on the AC string current. In SmHC, it is observed that the CAVC only has high impedance at 5^{th} and 7^{th} harmonics as shown in Fig. 3. VMMs are not participating in the harmonics mitigation as expected. This method will reduce the available operation margin of CAVC. As a consequence, the harmonics compensation will be limited by the operating margin of CAVC which is the main constraint of this method.

B. All-member harmonics compensation

Because of the mentioned constraint of the SmHC, the second method, All-member Harmonics Compensation (AmHC), is proposed. On the contrary of the first method, both CAVC and VMMs participate in the task. Since the inverters are connected in series, the current is flowing through all the inverters. Therefore, all the individual inverters can detect the distorted AC string current autonomously and participate in harmonics mitigation as presented in Fig. 4.

Adding harmonics compensator to VMM inverters does not impact the stability of the system and all the inverters provide high impedance at 5^{th} and 7^{th} harmonics as shown in Fig. 5. This method will lessen the burden on CAVC by using operating margin of VMMs. Consequently, operating range of the AC-stacked PV inverter architecture under grid background harmonics will be expanded. The detailed decentralized control and AmHC control scheme for the AC-stacked PV inverter architecture is presented in Fig. 6.

IV. RESULTS AND DISCUSSIONS

To verify the effectiveness of the proposed harmonics mitigation methods, CHIL test bed with a real-time power electronics simulator with 500ns time step [27] and a 150MHz digital controller is built.

The CHIL experiment results of harmonics mitigation controls with different grid background harmonics in nominal

Fig. 3: Impedance of individual inverter voltage disturbance to the string current in SmHC.

Fig. 5: Impedance of individual inverter voltage disturbance to the string current in AmHC.

Fig. 6: AC-stacked PV inverter control scheme with AmHC.
PV operating condition, PV1: 1000W/m², PV2: 1000W/m², PV3: 1000W/m², \( P_{PV\text{total}} = 726W \) and \( I_{string\text{RMS}} = 16.3A \), are presented in Fig. 7. When 8% of 5\(^{th}\) and 7\(^{th}\) grid background harmonics are added to the grid voltage, 9.5% and 6.5% of harmonics currents are caused without any harmonics mitigation control, respectively, as shown in Fig. 7a and Fig. 7b.

With SmHC under 8% of 5\(^{th}\) grid background harmonics, the duty cycle of CAVC is increased by 12% which is 41% of available operating margin (\( \frac{12\%}{29\%} \times 100 = 41.4\% \)). By applying the AmHC, all the inverters participate in the harmonics current mitigation by using their 4%-5% of additional duty cycle which is 13.8%-14.7% of available operating margin. As a result, the AmHC reduces the burden on the CAVC and increases the overall operating margin of the entire architecture for the harmonics mitigation, which can be significant when more modular inverters, VMMs, are stacked in series.

V. CONCLUSION

This paper investigated two control strategies for the mitigation of the influences of grid background harmonics in
the distributed grid-tied AC-stacked PV inverter architecture and evaluated their performance. In the first approach, only CAVC has high impedance at the selected harmonics. Consequently, the harmonics compensation will be limited by the operating margin of CAVC, which is the main constraint of this method. In the second approach, all the inverters, CAVC and VMMs, participate in harmonics current mitigation independently by utilizing their local AC current measurements and by having individual PR controllers, which are active at the selected resonant frequency. By applying AmHC under 8th 5th harmonics content, the operating margin for the harmonics compensation on the CAVC can be increased by 47%. Consequently, operating range of the AC-stacked PV inverter architecture under grid background harmonics can be expanded. This improvement will be more significant on the system where more VMMs are stacked to satisfy the high voltage requirement for grid-connection; where the CAVC may not be able to handle all the harmonics alone. Impedance analysis in the frequency domain and CHIL experiments were provided to show the effectiveness of the proposed methods.

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REFERENCES


