Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter

Available at: https://works.bepress.com/facultyofengineering_universityofmalaya/132/
Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter

Tan Kheng Suan Freddy, Nasrudin A. Rahim, Senior Member, IEEE, Wooi-Ping Hew, Member, IEEE, and Hang Seng Che, Member, IEEE

Abstract—Recently, reduced common-mode voltage (CMV) pulsewidth modulation (RCMV-PWM) methods have been proposed to reduce the leakage current in three-phase transformerless photovoltaic (PV) systems. However, most of these studies only focus on leakage current elimination and neglect the overall performance of the PV systems on issues such as cost, voltage linearity, dc-link current ripples, and harmonic distortion. In this paper, a three-phase transformerless inverter, adapted from the single-phase H5 topology, is investigated. Since the H5 topology has been conventionally developed for a single-phase system, its adaptation to the three-phase system requires the development of corresponding three-phase modulation techniques. Hence, modulation techniques are proposed based on conventional PWM. The performances of the proposed PWM, in terms of CMV, leakage current, voltage linearity, output current ripples, dc-link current ripples, and harmonic distortion are studied and discussed via simulation and experiment. It is proven that the proposed topology is able to reduce the leakage current without sacrificing the overall performance of the system.

Index Terms—Common-mode voltage (CMV), leakage current, photovoltaic (PV) system, transformerless.

I. INTRODUCTION

The rapid increase in human population and the fast growth of industries have shifted the attention of the research community toward photovoltaic (PV) energy. PV energy is free, green, and inexhaustible. Recently, PV power systems have become widespread due to the government incentives, reduction in PV arrays prices, and the advancement of power electronics and semiconductor technology [1]–[6].

Generally, there are two types of grid-connected power systems, i.e., with a transformer and without a transformer. The transformer used can be a high-frequency transformer on the dc side or a low-frequency transformer on the ac side [7]–[10]. In addition to stepping up the input voltage, it plays an important role in safety by providing galvanic isolation, which eliminates the leakage current and avoids dc injection into the grid. Nevertheless, the transformers are bulky, heavy, and expensive. Hence, transformerless PV systems are introduced to overcome these issues. They are smaller, lighter, lower in cost, and highly efficient [9]–[12].

However, safety is the main concern for the transformerless PV systems due to high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow from the PV to the grid. When the PV is grounded, stray capacitance is created. The fluctuating potential charges and discharges the stray capacitance, which generates high leakage current [13]–[15], [26]. In addition to the safety issue, the high leakage current will degrade the performance of the PV system by increasing the grid current ripples, losses, and electromagnetic interference.

Conventional pulsewidth modulation (PWM), either space-vector PWM (SVPWM) or discontinuous PWM (DPWM), are not suitable for three-phase transformerless PV applications due to high leakage current. In order to reduce the leakage current to meet the requirement of the standard, several conversion structures and modulation techniques have been proposed recently. In [5], the connection between the neutral...
TABLE I
PULSE PATTERNS FOR VARIOUS PWM METHODS

<table>
<thead>
<tr>
<th>Method</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
<th>A6</th>
</tr>
</thead>
<tbody>
<tr>
<td>SVPWM</td>
<td>573003</td>
<td>623037</td>
<td>234303</td>
<td>654564</td>
<td>765067</td>
<td>761067</td>
</tr>
<tr>
<td>AZPWM</td>
<td>623216</td>
<td>432134</td>
<td>234543</td>
<td>654346</td>
<td>456564</td>
<td>2165612</td>
</tr>
<tr>
<td>RSPWM</td>
<td>315313</td>
<td>315313</td>
<td>315313</td>
<td>315313</td>
<td>315313</td>
<td>315313</td>
</tr>
<tr>
<td>B1</td>
<td>21612</td>
<td>22123</td>
<td>47234</td>
<td>545245</td>
<td>654565</td>
<td>165616</td>
</tr>
<tr>
<td>NSPWM</td>
<td>21612</td>
<td>22123</td>
<td>43234</td>
<td>545245</td>
<td>654565</td>
<td>165616</td>
</tr>
<tr>
<td>DPWM</td>
<td>772127</td>
<td>230327</td>
<td>74347</td>
<td>45054</td>
<td>76567</td>
<td>601616</td>
</tr>
<tr>
<td>MDPWM</td>
<td>772127</td>
<td>23732</td>
<td>74347</td>
<td>45734</td>
<td>74547</td>
<td>65756</td>
</tr>
</tbody>
</table>

Fig. 2. Voltage vector states for the RCMV-PWM methods with different ways of partitioning the space-vector sectors. (a) Type A. (b) Type B.

point of the grid to the middle point of the dc link ensures constant voltage across the stray capacitance, which leads to zero leakage current. However, this is not practical because such connection creates the inductance in the neutral line. This inductance generates high-frequency potential between the PV array and the ground, which leads to leakage current higher than the permissible level recommended in the standard [17].

A new conversion topology has been proposed in [19] with extra two switches and 12 diodes. These excessive additional components significantly increase the cost, the losses, and the size of the entire PV system. Moreover, the leakage current is still relatively high (280 mA) [19].

Reduced CMV PWM (RCMV-PWM) methods such as active zero-state PWM (AZPWM) [20], near-state PWM (NSPWM) [21], and remote-state PWM (RSPWM) [22], have been proposed recently. Without zero vectors, RCMV-PWM methods are able to reduce the CMV to reduce the leakage current. Nevertheless, the overall performances in terms of voltage linearity, dc-link and output current ripples, line-to-line output voltage pattern, losses, and total harmonic distortion (THD) of the output current are degraded. Considering all criteria for the transformerless PV systems, this paper investigates a three-phase transformerless inverter, as shown in Fig. 1, by adapting the popular single-phase H5 topology [28] for three-phase operation. As shown in Fig. 1, an additional switch is added to the conventional three-phase inverter structure to provide galvanic isolation. Given that a total of seven switches are utilized, this topology is referred to as the H7 topology hereafter.

H5 topology was originally proposed in [28] to reduce the leakage current in single-phase transformerless PV systems. Although H7 is a simple extension from the H5 inverter, study on this topology is yet to be reported and is thus attempted here in this paper. Since the H5 topology has been conventionally developed for a single-phase system, its adaptation to the three-phase system (i.e., the H7 topology) requires the development of a corresponding three-phase modulation technique. Hence, modified DPWM (MDPWM) based on conventional DPWM is proposed here. The performance of the H7 topology with the proposed modulation techniques is compared with other available RCMV-PWM methods [20]–[22] in terms of CMV, leakage current, dc-link current ripples, output current ripples, and the THD of the output current. Discussions are done based on Matlab/Simulink simulations and further validated via experimental works. It is proven that the H7 topology with the proposed modulation techniques gives the best overall performance and is suitable for transformerless PV applications for 230-V (RMS) grid system.

This paper is organized as follows. Leakage current reduction methods via RCMV-PWM are first discussed in Section II. The H7 conversion structure with the proposed modulation techniques and the operation principles are presented in Section III. Simulation and experimental results are shown in Sections IV and V, respectively, to validate the performance of the various topologies. Finally, conclusion is made in Section VI to summarize the results and findings.

II. COMMON-MODE BEHAVIOR AND LEAKAGE CURRENT REDUCTION METHODS

Leakage current minimization is one of the most important considerations in transformerless PV inverters. In the past, various transformerless PV inverter topologies have been introduced, with leakage current minimized by the means of modulation techniques and conversion structure, which will be discussed in this section.

A. Modulation Techniques

Several modulation techniques, which are termed as RCMV-PWM, have been proposed recently as listed in Table I. The modulation techniques can be classified into two types: A [20] and B [21], [22], based on the way the space-vector sectors are partitioned, as shown in Fig. 2.

In AZPWM, the active vectors are complemented with two opposing active vectors to create zero vectors with equal time. In RSPWM, a group of odd active vectors (V1, V3, and V5) or even active vectors (V2, V4, and V6) is used to generate desired output voltage with constant CMV. NSPWM employs only three adjacent active vectors. Without using any zero vectors,
RCMV-PWM reduces the CMV to reduce the leakage current. The CMV ($V_{CM}$) of a three-phase PV inverter is expressed as [5], [18], [26]

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3}. \quad (1)$$

However, issues such as voltage linearity, harmonic distortion, and output voltage arise due to the elimination of the zero vectors. One common problem for RCMV-PWM methods is its bipolar line-to-line output voltage. In every switching transition, the voltage changes across the inductors from $V_{DC}$ to $-V_{DC}$. This doubles the voltage stress across the inductors to twice of the input voltage. Moreover, such output voltage pattern generates overvoltage transients [21], [23], [24], large current ripples across the inductors (eventually requires larger filters), and high switching losses [1], which reduce the overall efficiency of the entire system. Moreover, NSPWM and RSPWM are only applicable in limited modulation range. NSPWM operates linearly only for $0.61 < m < 0.907$, whereas RSPWM is only applicable for $m < 0.52$ (m is modulation index). Out of this range, leakage current generated is higher than that of conventional SVPWM. For RSPWM, very high input voltage is required to inject the real power to the grid. As a result, high operational losses and high THD occur, which require the use of large filters [22]–[25].

### B. Conversion Structure

When the transformer is removed, the galvanic connection between the PV and the grid allows the leakage current to flow. Thus, many studies have been done in [28]–[36] to design conversion structure, which provides galvanic isolation to reduce the leakage current. Either dc decoupling or ac decoupling methods are utilized to disconnect the PV arrays from the grid during the freewheeling period. The modulation techniques are also carefully designed with the corresponding conversion structure in order to generate the desired output voltage and to reduce the leakage current. Such topologies yield satisfactory overall performance. Nevertheless, most of the galvanic isolation topologies are found in single-phase PV inverters. For three-phase PV inverters, modulation techniques are much more complicated, and galvanic isolation methods are therefore difficult to be implemented.

### III. PROPOSED TOPOLOGY AND THE OPERATION PRINCIPLES

Based on the given analysis, a simple modified H7 inverter with a proposed PWM method (known as MDPWM) is investigated to reduce the leakage current without compromising the overall performance of the PV systems.

#### A. Proposed MDPWM

Conventional DPWM yields outstanding performances in terms of voltage linearity, switching losses, and THD of the output current [37]. However, such optimum performances of the DPWM are degraded in transformerless PV applications. DPWM generates high leakage current, which causes high current ripples. As a result, the THD of the output current also increases. In order to maintain the unique characteristic of DPWM, a MDPWM based on conventional DPWM is proposed here to reduce the leakage current.

Unlike RCMV-PWM, the proposed MDPWM uses both active vectors and zero vectors to program the output voltage. However, zero vectors ($V_0$ and $V_z$) produce high CMV (0 and $V_{DC}$). Instead of two zero vectors, proposed MDPWM uses only one zero vector ($V_z$). This ensures that the CMV takes only values of $V_{DC}/3, 2V_{DC}/3$, or $V_{DC}$ as indicated in Table II.

In every odd regions (B1, B3, and B5), the pulse patterns of MDPWM remains the same as in the conventional DPWM. The difference appears only in even regions where $V_0$ is replaced by $V_z$ in MDPWM. For example, as shown in Fig. 3(a), MDPWM uses $V_1, V_2$, and $V_5$ in region A1 ∩ B1. In region A1 ∩ B2, $V_1, V_2$, and $V_5$, (instead of $V_1, V_2$, and $V_0$) are used as shown in Fig. 3(b). Obviously, $V_5$ has replaced $V_0$. The same approach is applied to the rest of the regions, and the pulse patterns are listed in Table I. Thus, the CMV is reduced, varying from $V_{DC}/3$ to $V_{DC}$ in odd sectors and $V_{DC}/3$ to $2V_{DC}/3$ in even sectors, as shown in Fig. 3.

MDPWM is proposed to reduce the CMV by reserving the use of zero vectors. Zero vectors are important as they determine the output voltage patterns. The elimination of the zero vectors in RCMV-PWM reduces the CMV at the cost of generating bipolar output voltage, which gives overvoltage
transients and increased current ripples. On the other hand, MDPWM does not suffer from such problem as it generates unipolar line-to-line output voltage, as shown in Fig. 3. The main drawback of MDPWM is the simultaneous switching of two inverter legs, which leads to increased switching losses. However, applying MDPWM is the only condition to reduce the leakage current while maintaining the unique characteristic of DPWM.

It is worth noting that, ideally, the CMV should be kept at a constant value to eliminate leakage current, as in RSPWM. However, RSPWM suffers from the problem of a limited modulation region, which increases its dc-link voltage requirement and the corresponding losses. Here, the MDPWM does not maintain the CMV at a constant value as in RSPWM. Instead, it merely reduces the CMV, in a similar manner as the NSPWM and AZPWM. This reduction in CMV, while being able to reduce the leakage current, may not be sufficient to lower the leakage current enough to satisfy the current standard of 300 mA rms [17]. Hence, in the H7 topology, additional switch $S_7$ is utilized to provide galvanic isolation between the PV array and the grid during the freewheeling period to further reduce the leakage current. This is explained in the succeeding section.

**B. Operation of the H7 Conversion Structure**

When the transformer is removed from the inverter, it forms a direct path for the leakage current to flow between the PV and the grid. This happens during the freewheeling period when all the upper switches turn on or turn off at the same time. In other words, the freewheeling period is the moment when the zero vector is applied. Hence, an additional switch $S_7$ is added to the three-phase full-bridge inverter to provide galvanic isolation between the PV array and the grid during the freewheeling period. The circuit configuration of the H7 inverter is shown in Fig. 1.

MDPWM clamps each phase leg of the inverter to the positive of the dc-link voltage, whereas the other two phases are modulated at switching frequency. Fig. 4 shows the simplified equivalent circuit of the H7 inverter when both active vectors and zero vector are applied in region $A_1 \cap B_1$ where $S_a$ and $S_b$ are the equivalent single-pole double-throw switches for the half-bridge of each phase. Phase A of the H7 inverter is clamped to the positive dc-link voltage.

As shown in Fig. 4(a), when active vectors ($V_A$, $V_B$) are applied, $S_7$ is turned on to generate the desired output voltage, and the corresponding CMV becomes $V_{DC}/3$ and $2V_{DC}/3$, respectively. On the other hand, when zero vector $V_Z$ is applied, all the upper switches $S_1$, $S_3$, and $S_5$ are turned on and connected to the positive (P) of the dc-link voltage. At this moment, $S_7$ is turned off to disconnect the PV from the grid. Therefore, leakage current finds no path to flow, as shown in Fig. 4(b). $V_{AN}$ and $V_{DN}$ decrease, and $V_{CN}$ increases until their values reach the common point, i.e., $V_{DC}/3$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{IN} + V_{CN}}{3} = \frac{1}{3} \left( \frac{V_{DC}}{3} + \frac{V_{DC}}{3} + \frac{V_{DC}}{3} \right) = \frac{V_{DC}}{3}.$$  \hspace{1cm} (2)

The switching pattern and the corresponding CMV for both region $A_1 \cap B_1$ and $A_1 \cap B_2$ is shown in Fig. 3. In region $A_1 \cap B_2$, $S_7$ is turned on all the time to generate the desired output voltage. Voltage vectors $V_1$, $V_2$, and $V_3$ are used, and the CMV is $V_{DC}/3$, $2V_{DC}/3$, and $V_{DC}$, respectively.

The same principles are applied to all the other regions. Obviously, CMV reduces and varies between $V_{DC}/3$ and $V_{DC}$. In addition to the CMV reduction, galvanic isolation further reduces the leakage current. As a result, the H7 topology with the proposed MDPWM combines the optimum behavior for both DPWM and RCMV-PWM methods.

It is worth noting that voltage $V_{AN}$, $V_{IN}$, and $V_{CN}$ are impossible to reach the common point $V_{DC}/3$ during the disconnection of the $S_7$. In practical applications, they are floating and oscillating due to the switches’ junction capacitance and resonant circuit effects. This effect will be seen clearer in the simulation results shown in Fig. 5. In fact, this effect can be avoided using the CMV clamping branch, which has been proposed in [10],[29], and [30]. However, the CMV clamping for the three-phase system requires additional hardware configuration, which may add burden to the cost, efficiency, and complexity of the design for both hardware and software. The CMV clamping method is not within the scope of this paper and will be discussed in future work.

**IV. SCALAR IMPLEMENTATION OF MDPWM**

In this section, the implementation of the proposed MDPWM is discussed. The overall block diagram for the proposed PWM is shown in Fig. 5. It is simple and straightforward as in conventional PWM. It can be easily implemented using the scalar approach as follows:

$$V_{A} = V_{a} + V_{0} = m \sin(wt) + V_{0}$$ \hspace{1cm} (3)

$$V_{B} = V_{b} + V_{0} = m \sin(wt - 2/3\pi) + V_{0}$$ \hspace{1cm} (4)

$$V_{C} = V_{c} + V_{0} = m \sin(wt + 2/3\pi) + V_{0}$$ \hspace{1cm} (5)
where $V_a$, $V_b$, and $V_c$ are the original sinusoidal reference signals, $V_0$ is the zero-sequence signal, and $m$ is the modulation index. $V_0$ is calculated via the magnitude test as follows:

$$V_0 = |\text{sign}(V_{\text{max}})| (V_{\text{DC}}/2) - V_{\text{max}}$$  \hspace{1cm} (6)

where $V_{\text{max}}$ is the original sinusoidal reference ($V_a$, $V_b$, or $V_c$) with the maximum magnitude.

After the injection of $V_0$, the resultant modulation signals ($V_a^*$, $V_b^*$, and $V_c^*$) are then compared with a triangular carrier wave to generate the logic signals $S_a$, $S_b$, and $S_c$. These logic signals ($S_a$, $S_b$, and $S_c$) are the pulse patterns of conventional DPWM. In order to generate MDPWM with only one zero vector ($V_0$), simple logic operations are utilized to generate the desired gating signals ($S_a$, $S_b$, $S_c$, and $S_d$). In other words, the implementation of the proposed MDPWM is in the same manner as in conventional DPWM. Only additional simple logic operations are required.

V. PERFORMANCE ANALYSIS OF MDPWM

A. Simplicity of Design and Cost

Unlike RCMV-PWM methods, the implementation of the proposed MDPWM is simple and straightforward. This is because the AZPWM, NSPWM, and RSPWM methods require the simultaneous use of two different triangular carriers (up-down and down-up triangular carriers) [23]–[25], which needs an advanced digital signal processor (DSP), such as Texas Instrument's TMS320F28335 with an enhanced PWM module, for implementation. Hence, it is difficult to be realized on low-cost microcontrollers with limited carrier configuration flexibility. On the other hand, the proposed MDPWM method requires only one carrier (up-down or down-up) for all three of its phases. Furthermore, the implementation of the MDPWM is as simple as the conventional DPWM with only additional logic operations that can be digitally implemented into the DSP.

B. Line-to-Line Output Voltage Patterns

The elimination of the zero vectors reduces the CMV in RCMV-PWM, but it generates undesirable bipolar line-to-line output voltage. Zero vectors are important as it determines the line-to-line output voltage pattern. MDPWM inherits the unique characteristic of unipolar line-to-line output voltage by reasoning the utilization of zero vectors. In every PWM cycle, the polarity of the voltage remains the same. Overvoltage transients and PWM current ripples are reduced; thus, smaller filter inductors can be used.

C. Voltage Linearity

Each PWM modulation method has a specific linear modulation region. Outside this region, the overall performance in terms of the THD of the output current, current ripples, voltage magnitude, and common-mode behavior are degraded. Therefore, a wide linear modulation range is preferable. MDPWM maintains the superior voltage linearity characteristic of conventional DPWM. By injecting the zero-sequence signal,
is modeled with two capacitors of 220 nF, each connected between the PV terminal and the ground. The dc-link capacitor ($C_{DC}$) is 2mF. The ground resistance ($R_G$) is 11 $\Omega$. The filter is made up of three inductors $L_F$, each having a value of 5 mH. The load resistance is 100 $\Omega$, and the modulation index $m = 0.9$. For fair comparison, the switching frequency is selected such that all the modulation techniques have equal average switch commutation, i.e., SVPWM, AZPWM, and the proposed MDPWM are modulated at 10 kHz, whereas DPWM and NSPWM at 15 kHz. RSPWM is not taken into account due to its impracticality in grid-connected applications.

Fig. 6 shows the line-to-line output voltage waveforms and the output currents for various modulation techniques. As shown in Fig. 6(a) and (b), conventional SVPWM and DPWM generate unipolar line-to-line output voltage. Both AZPWM and NSPWM share the common bipolar output voltage waveform. As observed in Fig. 6(c) and (d), the output voltage varies from $+V_{DC}$ to $-V_{DC}$. This doubles the voltage stress across the inductors by twice of the input voltage. As a result, losses and current ripples double, which requires the use of larger filter inductors. The proposed MDPWM shares the similar characteristic of conventional DPWM. It generates unipolar output voltage, as shown in Fig. 6(e).

Fig. 7 indicates the common-mode behavior for various topologies. Due to the utilization of zero vectors, both SVPWM and DPWM have the poorest common-mode behavior. As shown in Fig. 7(a) and (b), the CMVs vary from 0 to $V_{DC}$; thus, high leakage currents are generated. This also explains why the output current ripples are higher than the other topologies, as observed in Fig. 6(a) and (b). Without any zero vectors, AZPWM and NSPWM are able to reduce the leakage current by reducing the CMV, varying from $V_{DC}/3$ to $2V_{DC}/3$, as shown in Fig. 7(c) and (d), respectively. Thus, the leakage currents are reduced. Similarly, the proposed MDPWM is able to reduce the leakage current due to the reduced CMV and galvanic isolation. The CMV changes depending on $S_T$. When $S_T$ is turned on, the CMV varies from $V_{DC}/3$ to $2V_{DC}/3$ and from $V_{DC}/3$ to $V_{DC}$, otherwise.

Fig. 8 shows the microscopic view of the CMV waveform for the proposed MDPWM. Instead of $V_{DC}/3$ and $2V_{DC}/3$, small oscillation with magnitude up to 100 V is observed in the CMV waveform. This oscillation occurs when $S_T$ is turned off to provide galvanic isolation during the freewheeling period. Practically, $V_{AN}$, $V_{BN}$, and $V_{CN}$ cannot reach the common voltage of $V_{DC}/3$ due to the switches’ junction capacitance and resonant circuit effects, as explained earlier.

VI. SIMULATION RESULTS

In order to verify the operation and the overall performance of the PV system, simulations are carried out, as shown in Fig. 1, using Matlab/Simulink. All the simulations are done based on the same parameters. The PV array is simulated with a dc voltage source of 600 V. The stray capacitance ($C_{PV}$)