Low loss configuration for integrated PIN-Schottky limiters

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The Schottky-PIN limiter provides better receiver protection than a PIN diode-only limiter because it has a ~10 dB lower limiting threshold; however, its insertion loss has a strong impact on the overall noise figure because it typically precedes the gain stages. The extra diode in the Schottky-PIN limiter results in higher loss than the PIN diode-only limiter. The main loss contributors are the diodes’ parasitic capacitances, which load the signal path. In addition, the use of low cost, plastic packaged diodes introduces substantially more loss than either bare chips or hermetically packaged diodes.

Aside from reducing diode parasitic capacitance by either stacking or mesa construction, limiter loss can be minimized using circuit techniques. The loading effect of the Schottky diode on the RF path can be reduced with either a high-impedance, quarter wavelength line or a directional coupler, but these passive components add to either the size or cost, and furthermore, they detrimentally increase the limiting threshold. A new design recently demonstrated that a PIN-Schottky limiter’s insertion loss can be improved by integrating the two discrete diodes’ parasitic capacitances into a lowpass ladder network. The ladder configuration preserves the low limiting threshold, but requires that the PIN diode have two anode connections.

Traditionally, the PIN-Schottky limiter is fabricated using separate diodes, but we recently combined two diodes in a SOT-323 package to achieve greater miniaturization and demonstrated its viability in a microwave limiter application. The three-pin package, however, limits the PIN diode to one anode connection (see Figure 1). To reduce the insertion loss of microwave limiters fabricated with this device, a lowpass configuration for absorbing the parasitic capacitances was devised. This article summarizes resulting performance improvements using the lowpass configuration in a 1.8 GHz limiter.
Military Microwaves

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HYBRID LIMITER WITH PIN AND SCHOTTKY DIODES

The PIN diode, which forms the signal-attenuating half of the limiter component, can be functionally described by its 1.5 μm I-layer and a 100 μm diameter.9 The first dimension determines the limiter’s turn-on threshold,10 transient response time,11 and spike leakage;12,13 whereas, the second dimension caps its power dissipation. The APLAC simulation parameters (see Table 1) complete the PIN diode description. The Schottky diode, which constitutes the signal detecting half of the limiter component, can be described by a 250 mV barrier height at 1 mA and a set of SPICE parameters (see Table 2).

Electrical connections between the diode chips and the package leads are made using a combination of conductive epoxy and bond-wires (see Figure 1). A low thermal resistance of 150°C/W, achieved by attaching the diode chips directly to the copper lead-frame, improves power dissipation. The package leads and bondwires contribute ~0.5 and ~1 nH, respectively, to the component’s equivalent circuit model. The plastic encapsulation adds ~73 fF parasitic capacitances across the diodes. Measured at the package terminals, the PIN and Schottky diodes’ zero bias capacitances at 1 MHz are ~0.9 and ~0.7 pF, respectively. When the two diodes are connected in parallel in the limiter circuit, they present a combined ~1.6 pF capacitance in shunt with the RF path.

EVALUATION FIXTURE

The evaluation fixture consists of a 30 mil thick FR-4 PCB containing two 50 Ω co-planar waveguide (CPWG) with ground transmission lines (see Figure 2). The first line is continuous, but the second line has a narrow gap in the middle. The PIN-Schottky diode pair mounted on the continuous line acts as an experimental control; the circuit arrangement, two diodes connected in parallel, is the one originally envisaged for this component. The second PIN-Schottky diode pair is mounted on the gapped line with its adjacent leads straddling the gap. The diodes’ capacitances form the shunt arms of a lowpass π network. A chip inductor L1, which bridges the same gap, forms the series arm. Following the norm for this class of limiter, the PIN diode side is defined as the signal input.

SIMULATION

Through simulation, L1 is optimized for minimum loss at the operating frequency. To model the PIN-Schottky diode pair, APLAC and SPICE parameters from Tables 1 and 2 are combined inside the symbol X3 in Figure 3a. The frequency of 1.8 GHz is chosen for evaluation because it is the device’s upper limit. Figure 3b shows that an inductance of 3.2 nH results in the lowest insertion loss (~0.4 dB), while the best return loss occurs at a slightly higher inductance of 3.4 nH. The physical realization uses a standard value of 3.3 nH from the Toko LL1608 series.

The limiter circuit containing the paralleled diodes is represented by the condition L1 = 0. A higher loss of 1.2 dB is obtained with the diodes mounted in parallel following the datasheet’s recommendations. The results include an estimated fixture loss of 0.25 dB.

EXPERIMENTAL RESULTS

Experimental results confirm im-
proved performance of the π configuration over the parallel connection (see Figure 4). After 0.25 dB of fixture loss is removed from the raw data, a 0.9 dB difference is recorded between the two configurations at 1.8 GHz. Despite optimization at 1.8 GHz, improvement is maintained over a 1 GHz bandwidth.

The π-configured limiter is also significantly less reflective than the parallel-connected ‘control’ (see Figure 5). At 1.8 GHz, the π configuration achieves ~13 dB lower return loss than the control. The largest improvement occurs at ~2.4 GHz or ~33 percent higher than the design frequency, although we are not able to explain the responsible mechanism.

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cascaded limiter and low noise amplifier (LNA) confirms the \( \pi \) configuration’s lower loss. The test setup replicates the configuration of a limiter to protect an LNA input. The 1.8 GHz LNA uses a MGA-634P8 GaAs ePHEMT MMIC\(^6\) and has a ~0.5 dB NF at its connectors.\(^7\) The first combination of \( \pi \) limiter and LNA achieves ~1 dB NF, whereas, the second combination consisting of a parallel limiter and the LNA is significantly noisier at ~2 dB NF (see Figure 6). The difference between the two can be predicted from the limiters’ insertion loss. In a final product, the cascaded NF should be < 0.8 dB because the limiter fixture and the SMA ‘through’ adapter add ~0.25 dB loss to the experimental results.

The \( \pi \) configuration also outperforms the alternative loss mitigating scheme based on the ladder network.\(^6\) To ensure a fair comparison, the ladder-configured limiter is fabricated from the same PIN and Schottky diode chips as the \( \pi \) limiter, but the former’s diodes are assembled into separate SOT-323 packages so that its PIN diode can have the required dual anodes. At 1.8 GHz, the \( \pi \) configuration has ~0.2 dB insertion loss versus the ladder configuration’s ~0.4 dB (see Figure 7). Besides providing lower loss, the \( \pi \) configuration occupies approximately half the PCB space of the ladder configuration.

**CONCLUSION**

A 1.8 GHz limiter based on a three-pin hybrid Schottky-PIN diode component can benefit from lower loss and better matching when the diodes’ parasitic capacitances are configured into a \( \pi \) network, as compared to the manufacturer rec-

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\( \pi \) limiter exhibits 0.2 dB lower insertion loss than the ladder limiter at 1.8 GHz.
ommended parallel diode connection. Although demonstrated with an ASML-5822 PIN-Schottky diode pair, the proposed configuration has general utility. Since most packaged PIN diodes are available only in single-anode styles, (e.g. SOD-323, SOD-523, beam lead and glass diodes) and two anodes are required in the competing ladder configuration, the π configuration expands the number of usable devices. Moreover, the π configuration achieves lower loss than the ladder configuration when fabricated with a similar set of PIN and Schottky diode chips. Future work will investigate large-signal (limiting) and transient performance of the π configuration.

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References


