Limiting and transient performances of a low loss PIN-Schottky limiter

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Abstract — The main cause of loss in the PIN-Schottky limiter is the diodes’ parasitic capacitances. Techniques to counter the parasitic capacitances include using bare chip, air cavity packaging, diode stacking, mesa construction, isolating the Schottky diode from the signal path and connecting the diodes to a low impedance node. But the aforementioned techniques either sacrifice cost, manufacturability, size, performances or thermal ruggedness. To reduce loss in the PIN-Schottky limiter, we re-configured its parasitics into a low pass ladder network. This paper reports on the new configuration’s changed large signal and transient performances. We observed improved isolation at 0.9 and 2.4 GHz, and a beneficial reduction in the initial energy that slips through the limiter before limiting begins. In conclusion, this configuration simultaneously improves insertion loss, matching, isolation and spike leakage suppression. It has the potential to improve limiting performances in wideband receivers for wireless communication and medical imaging.

Index Terms — Limiter, receiver protection, Schottky assisted PIN limiter, Schottky enhanced PIN limiter, quasi-active limiter.

I. INTRODUCTION

The Schottky-PIN limiter improves receiver protection over a PIN diode-only limiter because the former’s limiting threshold is ~10dB lower [1]. Because the limiter usually precedes the gain stages in a receiver, its insertion loss can degrade the overall noise figure. The main cause of this loss is the diodes’ parasitic capacitances loading the signal path. Moreover, the extra diode in the Schottky-PIN limiter increases its loss over that of the PIN diode-only limiter. Limiter loss is further exacerbated by low cost plastic packaging for the diodes, such as the SOT-323.

Wideband limiters traditionally utilize bare chip diodes [2] - [3] or diodes in air cavity packages [4] in order to minimize parasitic capacitance, but are difficult to manufacture and are costly. Diode-stacking can also reduce the capacitance but adversely increases the turn-on threshold [5]. Removing part of the PIN junction area using mesa construction can reduce the parasitic capacitance but detrimentally increases the diode’s transient thermal impedance [6]. Alternatively, the Schottky diode can be isolated from the RF path with either a high-impedance quarter wave line [7] or directional coupler [8] - [9], but these passives add to either the size or the cost, and also increases the limiting threshold. The capacitive loading of the signal path can be reduced by connecting the diodes to a lower impedance (12.5 ohm) node [10], but the required impedance transformers are lossy and space-consuming. A well known technique to reduce loss in the PIN diode limiter is to absorb the diode capacitance into a low pass T network [2] - [11]. Recently, we demonstrated that absorbing the PIN-Schottky limiter’s parasitic capacitances into a low pass ladder network can substantially reduce the insertion loss over several GHz of bandwidth [12]. The ladder configuration has considerable advantages over previous techniques because it does not require additional component or space. This work builds on the previous one by investigating the configuration’s effect on the large signal and transient performances.

II. MATERIALS AND METHODS

This section first describes the diodes selected for implementing the limiter, then the PCB test fixture and finally, the measuring arrangement.

A. PIN and Schottky diodes

To minimize material cost, the limiter was designed around SOT-323 packaged diodes. A PIN diode with a 1.5um I-layer is selected to minimize transient response time, turn-on threshold and spike leakage. The PIN diode’s package has two anode connections formed by bonding two wires to the chip in opposite directions in order to minimize the mutual inductance (fig. 1). The zero bias capacitance measured at the package leads is ≤1pF [13].

The Schottky diode is characterized by a 250mV barrier height (at 1mA) and a ~0.8pF zero bias capacitance [14].

In both diodes, the parasitic inductances associated with the bond-wires and the leads are 0.7nH and 0.4nH, respectively [15].

B. Limiter assembly

The limiter was assembled on a 30mil thick FR4 PCB containing a 50Ω co-planar waveguide with ground (CPWG) transmission line with a gap in the middle. The PIN diode is mounted with its anode leads straddling the gap. The Schottky diode is connected to the output side of the transmission line as is usual for this class of limiter. The combination of a dual-anode PIN diode, a Schottky diode, and a gapped line results in a small signal equivalent circuit that approximates a low-pass ladder filter.
For performance comparison, a conventional PIN-Schottky limiter was assembled from a similar diode combination on a continuous transmission line on the same PCB. Since both diodes are paralleled in the conventional limiter configuration, its small signal equivalent circuit can be approximated by a shunt capacitor with a value equal to the total of the two diodes’ capacitances, or 1.8pF.

C. Measuring arrangement

The limiter’s small signal characteristics are measured on a network analyzer (VNA) which source power is adjusted to -20 dBm to avoid limiting. After a 2-port calibration at the test cable ends, the fixture is removed from the results using normalization.

The saturated limiter approximates a short which will manifest as an unusual dip in the swept power result. So, the test setup incorporates an isolator and an attenuator to buffer against the impedance mismatch (fig. 2).

![Fig. 1 Details of the PIN diode construction (top right), the limiter assembly (top left), and its small signal equivalent circuit (bottom right)](image)

![Fig. 2 This swept power test setup is designed to buffer the test equipment from the large mismatch presented by the saturated limiter](image)

The limiter’s transient response is evaluated using a ten microsecond burst of 30dBm 900MHz carrier (fig. 3). The energy content of the burst is, \( P(W) \times t(s) = 10^{-9}J \).

![Fig. 3 transient response test setup at 900MHz](image)

III. RESULTS AND DISCUSSION

The low pass ladder configuration clearly improves the insertion loss toward the upper end of the frequency range. The normal configuration has a 1.7GHz bandwidth at the -1dB loss point. The ladder configuration extends the -1dB bandwidth to 3 GHz – or a 76% increase (fig. 4). The ladder configuration’s loss at 3 GHz is ~0.9 dB better. Although not shown, the ladder configuration also improves the return loss over the evaluated bandwidth.

![Fig. 4 The significant loss reduction in the ladder configuration increases the limiter bandwidth at the -1 dB point from 1.7 GHz to 3 GHz or 76% higher](image)
Isolation at 2.4 GHz is improved by as much as 6 dB and also exhibit a faster rate of change (fig. 6). Additionally, the ladder configuration beneficially shifts the beginning of the isolation plateau (saturation) from 10 dBm to 20 dBm. The ladder configuration shifts the limiting threshold up by ~5 dB, but this should not be a serious performance impediment. Isolation at 2.4 GHz is improved by up to 6 dB at 2.4 GHz

The ladder configuration’s isolation is consistently ~5 dB better than the normal configuration throughout 0.9-2.6 GHz (fig 7). It is possible that the 5 dB difference will be maintained below and above this frequency range but this was not investigated. The two configurations’ different isolation performances can be explained by the alignment of their package parasitic inductances with respect to the signal path (fig. 8). In the ladder configuration, these inductances are in series with the RF path and they form a voltage divider with the saturated PIN diode’s low impedance. In comparison, the normal configuration’s parasitic inductance is in series with the PIN diode’s junction resistance and this retards isolation.
VII. CONCLUSION

Configuring the Schottky-PIN limiter as a ladder network in order to improve its small-signal insertion loss changes its large signal and transient responses. The ladder configuration has significantly better isolation and spike suppression than its normal counterpart. The latter two improvements further enhance the limiter’s ability to protect sensitive devices. Alternatively, the substantially improved isolation may allow the designer to cut down the number of limiter stages for cost saving. We anticipate little or no objection to its adoption in commercial products because no extra cost or space is involved, whereas the improvements are tangible. We anticipate the loss reduction enabled by this configuration will improve the sensitivity of wireless communication and medical imaging. One interesting idea for a new product is to integrate both diodes and the ladder network into a 4-terminal package such as the SOT-343.

Fig. 9 The ladder configuration beneficially reduces the energy that slipped through the limiter at the beginning of the impulse or the spike leakage.

Fig. 10 Output power (Po) and attenuation (A) vs. input power (Pi) at 1.8 GHz

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APPENDIX: ADDITIONAL RESULTS

The ladder configuration demonstrates significantly better insertion loss and isolation performances than its normal counterpart at 1.8 GHz (fig. 10).

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