Wideband voltage variable attenuator with fewer components

Chin-Leong Lim
The cellular infrastructure equipment is subject to intense pricing and size pressures. Recently, a Rubik’s Cube size base station has been demonstrated.\textsuperscript{1} Both cost and size can benefit from reducing the number of circuit elements in a function block. Low noise amplifiers (LNA), fabricated using contemporary semiconductor technologies, have some degree of gain variability. For example, 0.9/1.9/2.5 GHz LNAs, fabricated on 0.25 μm GaAs enhancement mode pseudomorphic (EPHEMT) process, require 3 dB gain specification windows.\textsuperscript{2-4} In critical applications, voltage-variable attenuators (VVA) are required for gain leveling. Some contemporary LNAs for base station applications have dedicated ports for connecting to external VVAs (see \textbf{Figure 1}).

PIN diodes, configured as the PI or the bridged-TEE topologies, are commonly used for realizing wideband, high linearity and compact VVAs. The commercial availability of pre-configured diode arrays,\textsuperscript{5,6} and standalone modules\textsuperscript{7} can minimize the design effort and space requirement. These PIN diode VVAs typically contain 14 to 18 circuit elements each (see \textbf{Table 1}) and these numbers have remained constant for two decades. So, a tantalizing route to size and cost reduction lies in reducing this quantity. Another argument against employing conventional topologies is that they typically have more than 30 dB of dynamic range (DR), whereas gain alignment requires far less.

Aiming at drastically reducing the cost of implementing the VVA function, a variation of

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{vva_diagram}
\caption{Block diagram of an LNA module with provision for connecting an external VVA.}
\end{figure}

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the TEE topology that utilizes only one variable element has been explored. Although it has a significantly reduced DR, it is, nevertheless, sufficient for gain alignment. This article describes the design and construction of the variable resistance circuit, as well as its modeling and performance.

**TEE VVA Topology**

The new VVA configuration evolved from the fixed TEE attenuator (see Figure 2). For a specific characteristic impedance \( Z_0 \) and attenuation \( A \), TEE attenuator’s series \( R_s \) and shunt \( R_p \) resistors are given by:

\[
R_p = \left( \frac{2}{\sqrt{Z_0}} \right) \cdot 10^{\frac{A}{10}} \left( 10^{\frac{A}{10}} - 1 \right)
\]

\[
R_s = \frac{\left( 10^{\frac{A}{10}} + 1 \right) \cdot Z_0}{R_p}
\]

VVAs rarely are based on the TEE topology because all three resistors must be varied simultaneously to keep \( Z_0 \) constant. Instead, a variation known as the bridged-TEE is more popular because only two resistances need to be varied. A proposed modification to the TEE topology, whereby only \( R_p \) is varied, works on the premise that \( Z_0 \) deviates minimally for small excursion in the value of \( R_p \). As a larger change in \( R_p \) will skew \( Z_0 \) from the system reference impedance, the dynamic range is limited by the worst return loss that can be tolerated. When the required dynamic range is relatively small, the proposed configuration can advantageously replace conventional topologies for component reduction. Although the narrowband attenuators, like the hybrid coupled and the resistive line, can also achieve low component count, they are either expensive or require a large PCB area. The variable resistance can be chosen from either field-effect transistor (FET) or PIN diode and the entire VVA can be fabricated in monolithic or discrete forms. It is possible that this configuration is not new because it is so simple, but a literature search did not unearth any similar work. The value of \( R_s \) determines the compromise between minimum attenuation and dynamic range (see Figure 3). As previously discussed, the dynamic range is limited by the increasing impedance mismatch for larger deviation of \( R_p \) and so, a return loss limit of 10 dB was used as the constraining parameter in the simulation. The simulation also assumes ideal components.

**VARIABLE RESISTANCE ELEMENT**

Although either a FET or PIN diode can function as the variable resistances, the optimal technology will depend on the application. For example, the former’s microAmp-level operating current will be clearly advantageous in battery-powered equipment. Whereas in mains-powered equipment, such as cellular base stations, the latter’s high linearity will be more useful than power saving. A PIN diode with the following salient characteristics – 125 \( \mu \)m I-layer thickness and 1500 nS carrier lifetime – was selected to realize the VVA, because it has the highest linearity in the diode portfolio.

A dual cathode SOT-323 pack-

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**TABLE 1**

Comparision of the number of circuit elements in various compact, wideband VVAs

<table>
<thead>
<tr>
<th>Topology</th>
<th>No. Circuit Elements</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Active</td>
</tr>
<tr>
<td>3-diode Pi</td>
<td>4</td>
</tr>
<tr>
<td>Waugh 4-diode Pi</td>
<td>4</td>
</tr>
<tr>
<td>Bridged TEE</td>
<td>2</td>
</tr>
<tr>
<td>This Work</td>
<td>1</td>
</tr>
</tbody>
</table>

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**Fig. 2** Fixed TEE (a), bridged TEE (b) and one variable resistance TEE (c) attenuators.

**Fig. 3** Dynamic range and minimum attenuation vs. \( R_p \).

**Fig. 4** Simplified circuit of the HSMP-481 dual cathode PIN diode.
up to approximately 1.1 nH. However, when the two bond-wires are arranged such that their currents flow in the opposite directions, the resultant mutual inductance, M, lowers the effective bond-wire inductance to \((L_b - M)/2\). So, the actual total inductance could be considerably lower than the simple calculation, which did not account for mutual inductance.

For linear structures, such as two straight wires separated by "d" and of a height "h" above ground, M can be determined analytically from:

\[
M \approx \frac{\ln h}{d} \left(1 + \left(\frac{2h}{d}\right)^2\right)
\]  

Unfortunately, M cannot be easily determined for bond-wires because the height changes along their length (usually referred to as "loop profile"). Since it is necessary to account for the bond-wires equivalent inductance in the simulation, a value of 0.35 was assumed for M; the value was chosen without any expectation of accuracy.

### ASSEMBLY AND MODELING

To achieve the target DR of approximately 4 dB, an Rs value of 5.1 Ω was selected for the evaluated circuit (see Figure 5). The 0.8 mm thick FR-4 PCB was designed for a different project and so has many unused pads (see Figure 6). The microstrip traces associated with the VVA input and output connections are dimensioned for a 50 Ω characteristic impedance. The value of L1, which chokes the DC bias, was chosen to suit the 2 GHz upper frequency limit. A multilayer inductor was chosen to save cost because preliminary simulation with a higher Q inductor (such as wirewound) showed insignificant improvement (∼0.03 dB) in circuit loss. Figure 7 shows the simulated minimum attenuation versus L1’s unloaded Q, excluding the PCB and connector losses. The arrows mark the published typical Q at 1.8 GHz for Toko LL1608 wirewound inductor and Coilcraft 0603CS multilayer inductor. Table 2 is the part list of the 1-diode TEE VVA.

The VVA was modeled so that its
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**RESULTS AND DISCUSSION**

The experimental results at the nominal cellular frequencies of 870 MHz and 1.85 GHz are > 4.5 dB dynamic range, –1.5 dB minimum attenuation and +53.5 dBm third order intercept point (OIP3). The simulation and measurements agree reasonably. The measured attenuation changes from –1.5 dB to –6 dB at 870 MHz when the current is swept over a 0 to 1.6 mA range – the current is constrained to this range to ensure better than a 10 dB return loss (see Figure 9). A comparable PI VVA needs 0 to +10 mA operating current and has a minimum attenuation of –4 dB. When cascaded with an LNA, the improved minimum attenuation limit (e.g., –1.5 dB vs. –4 dB) is less degrading to the performances could be evaluated in a linear simulator. The models nest in a 3-level hierarchy shown in Figure 8: the complete PCB assembly at the top (a), the packaged diode in the middle (b) and the diode equivalent resistance at the bottom (c). The RLC equivalent circuits comprise only the first-order parasitic and are created after the Rhea intuitive method of whittling away lesser parasitic. Specifically, the resistors’ predominant parasitic (Lpst) was decided using a rule and the value was guesstimated. The inductor L1 parasitic capacitance Cpst was calculated from the self resonance frequency specified by the manufacturer. The diode package model follows the SOT-323 model published by the manufacturer, but additionally accounts for lower bond-wire inductance, due to mutual inductance. The current dependent resistance follows the APLAC linear representation of the HSMP-381x PIN diode.

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**Fig. 8** Nested models of (a) complete VVA, (b) packaged diode and (c) diode current-controlled resistance.

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**Fig. 9** Simulated and measured attenuation and return loss vs. diode current at 870 MHz.
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Also assumes that the current is limited to 0 to 1.6 mA to ensure better than a 10 dB return loss (see Figure 10). The maximum simulation errors are 1.2 and 2 dB for attenuation and return loss, respectively.

The OIP3 is as high as for the PI topology’s. Using 869 and 871 MHz input signals at 25 dBm, the OIP3 decreases in an almost 1-to-1 manner with increasing attenuation but remains above 53.5 dBm (see Figure 11). The OIP3 at 1.85 GHz was not measured, but is expected to be higher, because it has been previously reported that a silicon PIN diode’s OIP3 increases linearly with frequency.26 The distortion is caused by RF currents modulating the I-layer’s charge density. So, the distortion increases with attenuation because a larger fraction of the RF currents is diverted from the load to the diode.

CONCLUSION

The 1-diode TEE VVA contains only one-third of the total components in the equivalent PI and bridge-TEE topologies, but can fulfill the same gain-leveling role. Additionally, it is capable of lower attenuation than a PI VVA built with similar diodes, has comparable linearity and yet operates at the fraction of the current. The much-improved minimum loss limit will benefit the cascaded noise figure. A simple design chart has been provided for designing to different dynamic range and minimum attenuation targets.

Beside the PIN diode, the FET is equally suited as the variable element. In fact, implementation in monolithic FET technology should result in the lowest cost and size. While the design is presented in the context of cellular LNA gain alignment, it should find use in other applications that do not require the conventional VVAs large dynamic range, such as automatic level control in power amplifiers and signal generators.

It is anticipated that the proposed configuration will lead to improvement in the base station LNAs size, cost, power consumption and sensitivity.

ACKNOWLEDGMENTS

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APPENDIX: THIRD ORDER DISTORTION MEASUREMENT

High IP3 is generally difficult to measure due to the great difference between fundamental and intermodulation amplitudes. Depending on the attenuator's setting (see Figure 12), the intermodulation products could either be overshadowed by the spectrum analyzer's internally generated distortion or have insufficient margin from the noise floor. Additionally, cross modulation between the signal sources can create artifacts that are indistinguishable from the real distortion. A tutorial lists the necessary hardware and procedures for enhancing measurement accuracy. To ensure that the setup used for the VVA evaluation did not contribute to the intermodulation results, its IP3 was measured at 62.8 dBm (versus the VVA's best case OIP3 of 58 dBm).

References
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