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PIN Switch Protects LNA from Overloads

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**PIN Switch Protects LNA From Overloads**

A MMIC low-noise amplifier (LNA) can be paired with an external PIN diode bypass switch to provide overload protection for mobile television receiver applications at 47 to 870 MHz.

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Receiver front ends for mobile television must provide the sensitivity needed to operate at far distances from a transmitter, but must provide overload tolerance when in the presence of large signals. Mobile television receive capability, which will be integrated into a large number of portable electronic devices, including cellular handsets, portable digital assistants (PDAs), laptop computers, and in-car-entertainment (ICE) systems, must provide good performance even as a user’s distance changes with travel, unlike traditional broadcast television. A low-cost solution to achieving high front-end mobile television receiver sensitivity with overload protection combines a high-gain low-noise amplifier (LNA) with a PIN diode bypass switch.

Most practical approaches to implementing mobile television receivers rely on reducing receiver gain in the presence of large signals. Varying RF signal gain eases the linearity requirements for the mixer stage, allowing the use of low-cost radio-frequency integrated circuits (RFICs) to create the receiver module. In the cascade analysis of a receiver front end with switchable or adjustable gain (Fig. 1, Table 1), the input third-order intercept (IIP3) improves as a function of the gain change. A receiver with adjustable gain handles large signals better than a receiver with fixed gain.

Automatic-gain-control (AGC) circuitry is also used to vary LNA gain, and because it is typically implemented prior to the channel filters, it can respond to overloads from adjacent-channel transmissions.

One way to reduce RF gain is to shunt part of the RF signal to ground prior to the LNA [Fig. 2(a)]. This approach uses a minimal number of RF switch elements but, when the switch is closed, causes an impedance mismatch that can affect other portions of the system. A variation involves connecting the damping element to the high-impedance or “hot” end of the LNA’s parallel resonant network, although this sacrifices RF selectivity prior to the LNA for the sake of a larger gain-control range.

Alternately, it is possible to bypass the LNA stage with a pair of RF switches when a received signal overloads stages following the LNA, such as a mixer or intermediate-frequency (IF) amplifier. During bypass operation, input signals are directly routed to the frequency downconverter IC [Fig. 2(b)]. As long as the components in the bypass signal path are matched to the characteristic impedance (75 Ohms in mobile television), mismatches will be minimized. Of course, adding the switches also adds to the circuit complexity.

In yet another approach, RF gain is lowered by decreasing the quiescent current to the LNA’s active device [Fig. 2(c)]. Amplifiers and devices based on this technique, such as dual-gate MOSFETs, use additional

<table>
<thead>
<tr>
<th>Input signal</th>
<th>LNA gain (dB)</th>
<th>Total gain (dB)</th>
<th>Total output IP3 (dBm)</th>
<th>Total input IP3 (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weak</td>
<td>20</td>
<td>30</td>
<td>-5</td>
<td>-25</td>
</tr>
<tr>
<td>Strong</td>
<td>0</td>
<td>10</td>
<td>-5</td>
<td>-5</td>
</tr>
</tbody>
</table>

**Table 1. Gain and IP3 values for the receiver front-end in Fig. 1**
device terminals for controlling the bias current. This gain-control method has the lowest circuit complexity since switching elements are not used, but suffers from degraded linearity as the collector/drain current is reduced below the nominal device DC operating point.9

To meet a customer’s requirements (Table 2) for an LNA for a dual-mode (analog/digital) mobile television receiver in the 47-to-870-MHz range, several MMIC options were considered, but disregarded for their inadequate linearity. Using a wideband high-linearity MMIC LNA (model MGA-68563) and an external PIN diode switch, a solution was developed.

The single-stage GaAs pHEMT LNA uses devices with gate width of 800 microns (Fig. 3). The device gate is connected to an internal current mirror to compensate for process variations and to minimize the effects of threshold voltage variations. The LNA employs lossy negative feedback for stability and to flatten the amplitude response within a 3-dB window from 100 MHz to 1 GHz.10

With its internal feedback and better than 10 dB output return loss, the MMIC didn’t require output impedance matching. But matching the input of the MMIC for such a broad frequency range (47 to 870 MHz) proved difficult and required an unconventional approach in which the FET drain current, Ids, is varied above the nominal 10-mA value to optimize the input return loss. The required input return loss performance was met with 20 mA Ids, but a value of 30 mA was chosen to allow enough margin for any degradation by the addition of the PIN diode switching circuit. Pin 4 on the MMIC LNA controls the current flow through the internal bias generator via external resistor R1 [Figs. 3(a) and 4(b)]; altering the dimensions of R1 changes Ids while the supply voltage Vd remains fixed at 3 V. The 300-percent increase in nominal Ids provides higher linearity.

In designing the LNA/switch circuit, the first iteration required four PIN diodes for the bypass switch [Fig. 5(a)]. It is a common configuration for a double-pole, double-throw (DPDT) switch. The circuit operates by turning on the upper pair of PIN diodes while the lower pair is zero biased, and vice versa. During normal operation, only the lower PIN diode pair is turned on and the RF signal is amplified by the LNA. When RF gain must be reduced, the upper PIN diode pair is turned on and the RF signal is routed around the LNA in bypass mode. The resistors are used to regulate the PIN diodes’ forward current and to isolate RF signals from the logic control ports VSW1 and VSW2. This first iteration required a high component count, so a simpler solution was sought.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA gain (dB)</td>
<td>15 ~ 20</td>
<td>18.5 ~ 21</td>
</tr>
<tr>
<td>LNA noise figure (dB)</td>
<td>&lt;1.3</td>
<td>0.8 ~ 1.3</td>
</tr>
<tr>
<td>LNA IIP3 (dBm)</td>
<td>≥ 6</td>
<td>9.5 ~ 12.5</td>
</tr>
<tr>
<td>Bypass loss (dB)</td>
<td>&gt; -5</td>
<td>-3.8 ~ -4.5</td>
</tr>
<tr>
<td>bypass IIP3 (dBm)</td>
<td>≥ 20</td>
<td>&gt; 20</td>
</tr>
<tr>
<td>LNA current Id (mA)</td>
<td>&lt; 200</td>
<td>30</td>
</tr>
</tbody>
</table>

Test frequency range: 47 - 870 MHz.
Working with customer feedback, a simpler double-pole, single-throw (DPST) switch arrangement was developed [Fig. 5(b)] in which only the bypass path is connected or disconnected from the input and output ports. Because the LNA path is no longer switched in or out, the LNA supply ($V_{dd}$) must be turned off during bypass mode to make use of the intrinsic isolation of an unbiased FET. This approach degrades the return loss of the bypass path, due to this path having the shunt finite gate and drain impedances of the unbiased FET.

In normal operation, the supply to the PIN diodes is turned off ($V_{SW} = 0$ V) and the supply to the LNA is restored to 3 V. But these zero-biased PIN diodes suffer some parasitic capacitance that allows higher frequencies to pass. As a result, the LNA gain and return loss are degraded by incomplete isolation of the bypass path from the input and output ports.

In the LNA/switch, inductors L1 and L2 are ferrite beads that present high impedances over the full range of the biasing networks for the MMIC and diodes [Fig. 5(b)]. Without L1 as a choke, part of the input signal will be shunted to ground via resistor R3’s parallel-connected parasitic capacitance. Measurements made on a prototype without L1 verify that the inductor prevents degradation in the LNA’s noise figure. Capacitors C3, C4, and C5 decouple RF signals from the DC supply and are sized for low reactance ($X_c \leq 5$ Ohms at the lowest operating frequency. Capacitors C1 and C2 provide DC blocking at

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4. Plots show input return loss as a function of $I_p$ (a) and the relationship between bias resistor R1 and $I_p$ (b).
the MMIC input and output. A small value is deliberately chosen for C2 to create a highpass response that can compensate for the MMIC’s intrinsic gain rolloff at high frequencies. Resistors R1 and R2 control the MMIC supply current and are sized for 30 mA at a \( V_{dd} \) of 3 V. Resistors R3, R4, and R5 limit the PIN diodes’ forward bias to about 2.5 mA per diode at \( V_{SW} \) of 3 V. [Please contact the author for a component value list for Fig. 5(b).]

The circuit could be further simplified by using only one PIN diode. There is no advantage in this, however, since a diode pair occupies the same SOT-23 or SOT-323 surface-mount package as a single diode, with negligible price difference. The pair of diodes also offers some advantages: the series connection cuts half the parasitic capacitance and, since the even-order harmonics generated by the anti-series pair of PIN diodes are out of phase, they will cancel.12

To evaluate the LNA/switch performance, a prototype was assembled on a printed-circuit board (PCB) previously designed for a non-bypassed LNA application.13 The PCB consists of 10-mil-thick RO4350B laminate material from Rogers Corporation (www.rogerscorp.com), with a dielectric constant of 3.48 in the z-direction at 10 GHz.14 The PIN diodes and their associated biasing components were

5. The switching circuit was initially designed with four PIN diodes (a) and then modified to work with only two PIN diodes (b).
attached to the PCB by directly soldering them to the leads/pads of the earlier components. Two 1N5719 axial-lead glass diodes\textsuperscript{15} were used as the switching elements for D1. In a later PCB layout iteration, these diodes will be replaced by an SOT-packaged PIN diode pair (model HSMP-3893/E).\textsuperscript{16} The LNA’s median gain is 19.8 dB with a 1.3 dB variation within the frequency range of interest [Fig. 6(a)]. The frequency response is flattened by gently attenuating signals below 200 MHz by merit of the highpass response from small-valued DC-blocking capacitor C2. The gain rolloff at the upper frequency end is consistent with the MMIC’s characteristics and possibly due to negative feedback through the unbiased PIN diodes’ parasitic capacitance.

In bypass mode, the circuit exhibits 3.8 to 4.5 dB attenuation over the frequency range [Fig. 6(a)]. Loss in this mode is mainly caused by the parasitic series inductance of the PIN diodes. To a smaller extent, the loss in bypass mode is also affected by PCB dissipation, the FET terminal impedances of the FETs, and the parasitic parallel capacitance of resistor R4. Still, bypass mode losses were well within the customer’s -5-dB specification limit, so now attempts were made to reduce bypass losses further.

Both input and output return loss were consistently good (better than 17 dB) in bypass mode when evaluated across the specified frequency range. Return loss is primarily affected by how closely the unbiased FET gate and drain approximate open circuits. The return-loss performance is not
The noise figure was measured with and without ferrite bead inductor L1. The target noise figure specification (1.3 dB or less) cannot be met without L1. By comparing the traces, it can be surmised that signal loss attributed to the parasitic capacitance of resistor R3 is in the range of 0.3 to 0.6 dB, increasing the noise figure by the same amount. With L1, there is more in-band variation in noise figure (0.5 dB versus 0.2 dB), but this is not critical. The increased variation is likely caused by the ferrite bead’s progressively reduced choking capability with increasing frequency, especially above the 100 MHz or so self-resonant frequency (SRF) estimated from the manufacturer-provided performance graphs.  

The LNA’s output third-order intercept point was measured as several evenly spaced frequency points within the mobile television frequency band using a two-tone input power level of -20 dBm. The input third-order inter-