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Abstract. Planar memristive devices with bottom electrodes embedded into the substrates were integrated on top of CMOS substrates using nanoimprint lithography to implement hybrid circuits with CMOL-like architecture. The planar geometry eliminated mechanically and electrically weak parts such as kinks in top electrodes in traditional crossbar structure and allowed for the use of thicker thus less resistive metal wires as bottom electrodes. The planar memristive devices integrated with CMOS have demonstrated much lower programing voltages and excellent switching uniformity. With Moiré pattern, the integration process has sub-20 nm alignment accuracy, opening opportunities for 3D hybrid circuits for applications in the next generation memory and unconventional computing.

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1. Introduction

To sustain rapid progress in information technology in the post-CMOS (complementary metal-oxide semiconductor) era, there are intensive research efforts to go beyond Moore's Law in devices/materials, technologies, and architecture [1, 2]. Emerging devices based on novel physical properties such as spin, phase transition, and ionic charge transport are among the leading candidates for the next generation data storage and computing [3-5]. Resistive switching devices, which were linked to memristive devices or memristors, are non-volatile two-terminal electronic devices with variable resistance that depends on the history of applied voltage and current [6-9]. These devices have been proposed or demonstrated for a wide spectrum of applications such as random access memory [10, 11], implication logic [12], reconfigurable circuits [13, 14], and neuromorphic network [15, 16].

While totally replacing silicon based transistors with emerging devices might be formidable, a more realistic opportunity lies in nanodevices/CMOS hybrid systems, which takes advantage of the mature CMOS infrastructure and unique functionalities of the emerging devices. Some proof-of-concept demonstrations of the hybrid circuits have been reported previously. For example, hybrid ReRAM/CMOS circuits for memory application with 32Gb capacity [17] and 7.2 ns random-access time [18]. Memristors have also been integrated vertically with CMOS to implement FPGA-like functionality [13] to build circuits for data storage and neuromorphic computing applications [19]. However, the performances of the reported systems were not necessarily optimized. To improve CMOS compatibility and circuit reliability, memristive devices with lower programming voltages and better switching uniformity are needed. One approach is to confine conductive paths to limited locations inside of the switching materials by inserting Ru nanodots or another layer of materials [20,21]. Another approach is to engineer the device geometry, such as adopting a planar device geometry with bottom electrodes embedded in the substrate. The planar geometry eliminates kinks at the device junctions that are usually the electrical and mechanical weak parts and was reported previously to exhibit much better switching endurance [22]. It also reduces the variation of memristor cells and thus leads to better device performance uniformity. Furthermore, by using the planar structure, it is also possible to use much thicker thus less resistive electrodes. This is particularly attractive for the memristor/CMOS hybrid circuits where reduction of the RC delay and power consumption from the interconnects is of high priority.

In this study, we report the first demonstration on the integration of planar crossbar memristive devices with CMOS substrate, implementing CMOL (CMOS+molecular) architecture [23]. The planar devices with much thicker electrode exhibited much reduced programming voltages and enhanced switching uniformity. Furthermore, ON/OFF ratio larger than 10^4 was achieved for the planar devices using thicker electrode inside the hybrid circuits. The current work opened the opportunities of hybrid circuits that incorporate nanodevices with ultralow power CMOS circuits.

2. Experimental Methods

The CMOS chips used for this work were fabricated in a commercial foundry using a high-voltage (3.3 V) 0.5 μm technology. The wafer surface was finished with tetraethyl orthosilicate (TEOS) passivation and chemical mechanical polishing (CMP) so that the tungsten (W) vias were exposed. Planar memristor crossbars were then fabricated on top of the TEOS layer and made in connection with the W vias in CMOS circuitry through contact pads in the crossbar layer. NIL [24] was chosen for the integration because of its capability to pattern the whole coupon ($>1\text{ inch}^2$ area) with high resolution and relatively low cost.

To successfully integrate the planar memristor crossbars with CMOS in a monolithic way, two major fabrication challenges should be addressed. First, due to the dishing effect in CMP (tungsten was removed faster than TEOS), there was a 75 nm difference between the top of

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tungsten vias and the TEOS surface (Fig. 1, trace a). The non-flat surface was not favored by the NIL and extra considerations should be taken to enable the patterning over curved substrate. Second, deep trenches should be first etched into the TEOS layer and then back filled with thick metal electrode. As a result, dry etch processes with good etching profile and high selectivity to the resist mask should be developed.

Fig. 1 Atomic force microscope (AFM) characterization of the CMOS chip surface. (a) As-received CMOS chip after chemical mechanical polishing, with concave topography over the tungsten vias area. (b) After spin-coating the transfer layer. The topography of the transfer layer followed the contour of CMOS substrate. (c) After spin-coating the UV resist. The liquid UV resist planarized the surface. The uneven UV resist thickness raised challenges for NIL.

Bilayer resists were used in the fabrication process – an acetone soluble transfer layer and a UV cross-linkable liquid imprint resist layer. It was observed that the transfer layer generally followed the topography of the substrate (Fig. 1, trace b), while the liquid UV resist layer above has almost planarized the surface (Fig. 1, trace c). As a result, the residue UV resist layer variation after imprint would still be larger than 60 nm. Based on the observation, for the fabrication of planar bottom electrode, quartz mold with pattern height of 150 nm was duplicated from the master mold to overcome the residue resist layer variation after imprint. The molds designed for the integration contained arrays of 100 nm wide nanowires, each connected to a 10 μm by 15 μm contact pad. The contact pads had a grid structure (200 nm half pitch) that allowed for uniform resist flow during imprinting and metal penetration during the metal filling process. The integration process is schematically illustrated in Fig. 2. Since the residual UV resist layer after UV NIL was not uniform across the whole chip, the etching process of the residual UV layer, the transfer layer and the TEOS was critical in this integration process. We designed a controlled reactive ion etching (RIE) process in an STS ICP etcher. First, CF₄ plasma (30 sccm CF₄, 7 mTorr, 40 W ICP Power, 10 W Bias Power) was used to etch the residual UV resist with extra overetch to overcome the residue resist layer variation, and then O₂ plasma (30 sccm O₂, 7 mTorr, 40 W ICP Power, 10 W Bias Power) was used to etch away the exposed transfer layer. Finally, CHF₃/Ar based plasma etching (16 sccm CHF₃, 20 sccm Ar, 6 mTorr, 90 W ICP Power, 25 W Bias Power) was used to open the deep trenches into the TEOS layer. The etching recipe to open deep trenches in TEOS had high etching selectivity of TEOS to the resist (3:1) and thus we were able to etch 50 nm deep into the substrate, enabling the use of thicker bottom electrode to reduce the series resistance.

After the etching processes, Pd bottom electrodes were deposited in an electron beam evaporator to fill the trenches using the remaining resist stack as mask, followed by a lift off in acetone. The thickness of the metal electrodes was precisely controlled to be identical to the trench depth with less than 1 nm differences (as shown in fig. 4c). Next, a 20 nm thick TiO₂ switching layer was deposited onto the sample by sputtering (270 W RF Power, 10 sccm Ar, 20 sccm O₂, room temperature). The Pd/Ti/Pd top electrodes of the memristor arrays were patterned by a second nanoimprint lithography and followed by etching and metallization (Fig. 2b). The thin Ti layer was used to create oxygen vacancies at the Pd/TiO₂ interface [25] and 10 nm Pd on

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top of the Ti was used to protect the Ti layer from oxidation. Finally, because the sputtered TiO₂ layer blocked the connection of the top electrode to the W vias, a photolithography, etching and metal filling step was used to extend the W vias through the TiO₂ switching layer to reach the top electrodes (Fig. 2c). The top view of the contact pads, the W vias and the nanowires after each major fabrication step are schematically illustrated in Fig. 2d.

Fig. 2. Schematic illustration of the integration process. (a) 1st NIL on the CMOS substrate to make bottom electrode. (b) Sputtering the switching layer and 2nd NIL to make top electrode. (c) Additional steps to connect the top electrode to the paired W vias. (d) Schematic top-view of the pads and nanowires after a), b), and c), respectively.

3. Results and Discussion

3.1. Fabrication results

Fig. 3a shows the optical micrograph of the planar memristor crossbar arrays fabricated on top of the CMOS substrate. The planar memristors have 100 nm wide, 50 nm thick Pd bottom electrodes embedded in the TEOS passivation layer, 20 nm thick TiO₂ switching layer and 47 nm Pd / 3 nm Ti / 10 nm thick Pd top electrodes. Fig. 3b shows an SEM image of a 2 by 3 planar crossbar arrays with 100 × 100 nm² junction area inside the hybrid circuit. The thick bottom electrodes were completely embedded in the TEOS passivation layer and thus the fabrication crossbar memristors were planar. Fig. 3c shows a contact pad of the bottom electrode in a good contact with the W vias.

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Fig.3. Optical micrograph and SEM images of the integrated planar crossbar memristive arrays fabricated on top of the CMOS Substrates. (a) Optical image of a complete integrated hybrid circuits on one die of CMOS substrate. SEM images of (b) a 2 by 3 planar memristor array with $100 \times 100 \text{ nm}^2$ junction area **inside the hybrid circuit** and (c) the contact pad in good contact with the tungsten vias.

The planar device geometry of the fabricated memristive arrays was verified by AFM. Fig. 4a shows the AFM images of planar memristive devices and fig. 4b shows ribbed devices with bottom electrode (one wire laid horizontally in the image) fabricated above the TEOS plane. As we can see from the AFM images, the top electrode for the ribbed device was lifted up by the bottom electrode, while for the planar device with much thicker metal deposited, the bottom electrode was barely visible in the image (pointed out by two arrows)

Fig. 4. AFM images of (a) Planar memristor device with bottom electrode embedded in the TEOS layer (between the arrows) and (b) “Ribbed” memristor device with bottom electrode fabricated above the TEOS layer. (c) shows the cross-sectional profile of the bottom electrode. The scanned area is highlighted as the green line in (a). The height difference between the bottom electrode and the substrate surface was less than 0.6 nm, showing good control of the metal deposition process.

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3.2. Electrical measurements

To study the impact of device geometry on the electrical performance of the memristive devices, test crossbar memristive device arrays of different geometries were also fabricated on top of the CMOS substrate. The three device geometries were: ribbed and planar memristive devices with 14 nm and planar memristive device with 77 nm thick electrode. The thickness of the TiO_2 switching layer for the test devices was 35 nm. Thin Ti buffer layers were also used for all three device geometries to create oxygen vacancies at the Pd/ TiO_2 interface. We found that Ti was needed to put on the bottom electrode for the devices with thinner electrode to promote the adhesion to the TEOS substrate. For planar device with thicker electrode, bottom electrode without Ti layer was found to provide much better lift-off result, thus we put the Ti buffer layer on the top electrode. Two-wire measurement was used to characterize the performance of different devices (positive bias was always applied on the electrode with Ti buffer layer to form the device). Fig. 5 shows the switching behaviors of memristive devices with different geometries. For device with 14 nm ribbed bottom electrode (Fig. 5a), a 28V voltage was needed to form the device and the switching voltage was exceeding 10 V. In Fig. 5b, planar device with same electrode thickness (14 nm) only required 6 V to form the device and the switching voltage was reduced to around 4 V. Furthermore, by using much thicker electrode (Fig. 5c) together with the planar geometry, the forming voltage and switching voltage were further reduced to 3 V and 2 V respectively. The comparison of devices with three different geometries clearly showed that the use of planar geometry and thicker electrode greatly reduced the forming and switching voltages of the crossbar memristive devices.

Fig. 5. Comparison of switching behavior of non-planar and planar devices (a) Ribbed device (14 nm thick electrode, forming voltage (inset): 28 V) (b) Planar device (14 nm thick electrode, forming voltage (inset): 6 V). (c) Planar Device with thicker electrode (77 nm thick electrode, forming voltage (inset): 3 V). The planar geometry yields much lower forming and programming voltages. (d) Comparison of forming and switching voltages of different device geometry. The planar device geometry and thicker electrodes have contributed to the improved uniformity of switching behavior.

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In addition, the planar memristive devices demonstrated much improved switching uniformity. Fig. 5d shows the distribution of the forming and switching voltages of devices with different geometries. The switching voltages of the 77 nm planar devices were all at 2 V for the 16 tested devices, those for the ribbed devices varied significantly with a standard deviation of 2.93 V.

The lower switching voltage and better switching uniformity provided the memristive devices with much more flexibility for use in the hybrid circuits. For a conventional ribbed device, the top electrodes and switching layer were lifted up by the bottom electrode, which generated kinks at the corners of each switching junction [22]. The kinks changed the topography of the device structure, and were usually the electric and mechanic weak parts for the device junctions and electrodes. Associated with the intrinsic fabrication imperfections (such as line edge roughness and oxide thickness variation in the kinks), the ribbed device would expect more variations and defects than the planar device that would also contributed to the variation in electric field distribution and switching layer thickness variation and hence caused the non-uniform forming and switching processes of the ribbed devices. The planar device geometry eliminated the kinks so that the non-uniformity was greatly reduced.

At the meantime, the kinks generated a wavy top electrode for the ribbed device when it crossed multiple bottom electrodes (as shown in fig. 4b) and defects accumulated along the top electrodes further introduced variation in the series resistance of the ribbed electrodes. The high series resistance of the electrodes reduced the effectiveness of the switching and thus higher switching voltages were required for the ribbed devices. By using thicker electrodes, the series resistances on the wires were further reduced and led to even lower programing voltages. Furthermore, the use of thicker electrodes was also expected to be more defect-robust than the much thinner electrodes, which further improved the uniformity.

Fig. 6. Switching behavior of planar device with 50 nm thick bottom electrodes integrated with CMOS circuit. Both low switching voltage and high ON/OFF ratio were achieved that overcome the limitation of previous study in [13].

In the early demonstration using the same CMOS chip, the memristive devices were suffered from much larger switching voltages and lower ON/OFF ratio inside the memristor/CMOS hybrid circuits due to the high series resistance from the long routing interconnects inside the circuits [13]. By integrated planar memristive devices with much thicker electrode, both low voltage operation and high ON/OFF ratio were achieved. Figure 6 shows the planar device measured inside the hybrid circuits. For each memristor in the hybrid circuit can be accessed by a specially designed circuit on the same chip that controls the forming and switching of the devices before serving as the reconfigurable switch in the data routing network for logic gate arrays. The programming circuit had I/O ports that were connected externally to the

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measurement setup. The lower switching voltage and high ON/OFF ratio of the integrated memristive devices opened opportunity for use in much flexible CMOS circuits towards applications such as memory and neuromorphic computing.

3.3. Alignment for dense hybrid circuit.

In this study, cross and veneer patterns were used to align the bottom and top electrodes to the CMOS substrate. Optical image of the aligned veneer pattern of bottom electrode to CMOS substrate was shown in Fig. 7a. The golden patterns were located at the CMOS layer, while the silver patterns were from the bottom electrode. The veneer arrays at the four edges were designed with 500 nm pitch differences from the different layers. When the center pointer is aligned together, the overlay accuracy will be better than 500 nm. However, to fabricate hybrid circuits with much higher packing density using the area interconnection, smaller contact pads and dense wire arrays are necessary. As a result, the requirement for high accuracy alignment becomes a crucial task.

Fig. 7. Optical image of (a) cross and veneer alignment marks with 500 nm alignment resolution. (b) Fine alignment mark (Moiré pattern). (c) Magnified SEM image of Moiré pattern located at the area marked as * at the top left corner of (b), showing a 240 nm overlay.

The Moiré pattern can be employed for fine alignment. Fig. 7b shows an optical image of Moiré pattern on the CMOS chip after coarse alignment, showing a misalignment between the memristor arrays and the CMOS substrate. The overlay accuracy of this alignment was 240 nm, as verified by SEM images (Fig. 7c).

It is worth noting that Moiré pattern has the potential for sub-20 nm overlay in fine alignment [26]. Fig. 8 shows a set of simulation results demonstrating how the alignment mark moiré pattern changes with different overlay accuracy. Each Moiré pattern has two sets of gratings, one with 85 nanowires (1 μm pitch) and the other with 84 wires (1 μm + 12 nm pitch) so that the total widths of the two gratings are the same. The line widths of the gratings are all 300 nm. When the two sets of gratings are superimposed with each other with outer most nanowire aligned at two ends, due to the interference effect, the Moiré pattern will appear. In such case, since the outer nanowires are aligned better than the inner ones, it appears brighter in the outer part of the Moiré pattern. In the event of misalignment, the dark/bright pattern will shift depending on the amount of misalignment. The relative position of two sets of Moiré pattern can be used for fine alignment adjustment. A perfect alignment is shown in Fig. 8a, in which the center area is darer. As the overlay increases, the darker area will start to shift, as shown in Fig. 8b-8f). From the simulation results, it is possible to use this alignment mark to identify sub-20 nm overlay, as shown in Fig. 8b and Fig. 8c. In the current case, the Moiré pattern will show a periodic change of brightness with a period of 1 μm overlay (Fig. 8a and Fig. 8f). This is because the period of the Moiré pattern is $P1 \times P2 / |P1 - P2| = 84 \mu\text{m}$, which is exactly the width of the gratings.

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Fig. 8. Simulation of fine alignment mark using Moiré pattern with (a) perfect alignment, (b) 10 nm overlay (c) 20 nm overlay (d) 100 nm overlay (e) 500 nm overlay (f) 1 μ m overlay.

4. Conclusion

In this paper, we integrated the planar memristive device on top of the CMOS substrates using nanoimprint lithography. By carefully designed the process parameters, we were able to embedded 50 nm thick Pd bottom electrode into the TEOS passivation layer of the CMOS substrate. The integrated planar devices showed lower forming and switching voltages and much improved switching uniformity. The planar geometry also enabled the use of thicker electrodes for memristive devices, which further lowered the series resistance of the electrodes and both low programing voltage and high ON/OFF ratio was observed. Finally, we demonstrated that the integration process is promising for fabricating dense hybrid circuits with sub-20 nm alignment accuracy. The integration approach using the planar devices applies to various Memristor/CMOS hybrid circuits that can be used to implement next generation memory and unconventional computing applications.

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