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Low voltage resistive switching devices based on chemically produced silicon oxide

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We developed nonvolatile metal/SiO_x/Si memristive devices based on ultrathin (~ 1 nm) silicon oxide that was produced in a Piranha solution. The devices exhibited repeatable resistive switching behavior with low programming voltages (as low as 0.5 V) and high ON/OFF conductance ratio. Devices with active metals as top electrodes were bipolar switches, while those with inert metal electrodes were unipolar. We also studied the switching mechanisms for both types of devices based on the filament formation and rupture, and proposed conduction models for Pt/SiO_x/Si devices. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4817970>]

As CMOS (complementary metal-oxide-semiconductor) scaling approaches its limit, devices utilizing different physical phenomena have emerged. Resistive switches use high and low resistance states instead of charge storage to represent logic 0s and 1s. Recently, they were linked to memristors or memristive devices that were postulated by Chua four decades ago.^{1,2} Although Chua has recently defined any device that has a pinched hysteresis loop as memristor,³ there is an argument that the theory needs to be extended to address issues such as non-zero-crossing input-output characteristics.^{4,5} With advantages such as great scalability, fast switch speed, overwrite ability without erase, low power consumption, high endurance, and long data retention time, memristive devices are considered as a promising candidate for universal memory, unconventional computing, and beyond.^{6–11}

Being a two terminal device, a memristor is usually constructed by sandwiching a functional switching material in between two electrodes. Most memristive devices use materials such as transition metal oxides⁶ and perovskites as the functional switching layer.^{12,13} Unfortunately, not all of these materials are compatible with current silicon-dominated integrated circuits (ICs) industry. On the other hand, resistive switching phenomenon was discovered in amorphous silicon and silicon oxide more than 4 decades ago, and there is a revived interest in using these materials for memristors.^{14–25} Although compatible with CMOS technologies regarding materials and process, the reported programming voltages for silicon oxides based devices were too high (from 3.5 to 13 V)^{19,23,24} thus incompatible with the state-of-the-art low-power CMOS transistors in electrical operation.

In this letter, we report metal/SiO_x/Si based memristive devices exhibited repeatable nonvolatile resistive switching behavior with low programming voltages (as low as 0.5 V) and high ON/OFF conductance ratio. The ultrathin (~ 1 nm) SiO_x switching layer was produced in wet chemical processing using a Piranha solution. The device is either unipolar or bipolar depending on the choice of top electrode materials. We also studied the switching mechanism and explained the device behavior based on the formation and rupture of different type of conductive filaments.

During device fabrication, a highly doped prime grade silicon wafer (1–5 m Ω cm, p-type, (100)) was first dipped into 1:50 diluted hydrogen fluoric (HF) acid to remove the native oxide. The wafer was then treated in a Piranha solution (H₂SO₄:H₂O₂ = 3:1 volume ratio) for 20 min, during which a very thin layer (~ 1 nm) of silicon oxide (SiO_x) was produced on the silicon surface. Changes in the ratio of sulfuric acid to hydrogen peroxide to 5:1, and variance of the treatment time from 10 to 50 min, did not result in a different oxide thickness. This thin layer of SiO_x was used as the switching material for the devices. Finally, 12 to 24 nm thick disks (25 to 200 μ m diameter) of different metals (Pt or Cu) were deposited on the oxide surfaces as top electrodes using an electron beam evaporator through metal shadow masks. The deposition started with a base pressure of 7×10^{-7} torr, and the deposition rates were 0.2 and 1.0 $\text{\AA s}^{-1}$ for Pt and Cu, respectively. Each device consisted of a heavily doped silicon bottom electrode, a 1 nm thick SiO_x switching layer produced in the wet chemical process and a metal top electrode. The thickness of oxide layer was measured by a Gaertner LSE Stokes Ellipsometer. Surface chemical composition was analyzed using X-ray photoelectron spectroscopy (XPS) with a Physical Electronics Instruments (PHI) quantum 2000 XPS (monochromatic Al X-rays at 50 W with take-off angle of 15°). Electrical measurements were performed using a Keithley 4200SCS semiconductor parameter analyzer (SPA).

Figure 1 shows the Si 2p core level XPS spectra of the chemically produced SiO_x. Si⁰ (from the substrate) and Si⁴⁺ peaks dominated the spectra while only negligible amount of Si²⁺ was detected. The different abundance of Si²⁺ and Si⁴⁺ indicated that the Piranha produced silicon oxide is nearly stoichiometric (SiO₂), which is different with the RCA cleaning produced oxide.^{26–28}

An optical micrograph of a typical device arrays is shown in Figure 2(a). The device structure with IV characterization scheme is shown in Figure 2(b). During current-voltage (IV) characterization, the bottom electrode was grounded and voltages sweeps were applied to the top electrodes.

Figure 3 shows typical IV curves for devices with Pt and Cu top electrodes, which indicates that the switching behavior depended on the top electrode materials: devices with

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FIG. 1. X-ray photoelectron spectra data of Si 2p core level for wafer surface etched by $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2 = 3\text{:}1$ solution for 20 min. The result indicates that the produced silicon oxide is nearly stoichiometric, i.e., SiO_2 .

inert metal (Pt) top electrodes exhibited unipolar switching behavior, and the switching occurred on both polarity, while devices with active metal electrodes (Cu) were bipolar. The turn on voltage (V_{SET}) and turn off voltage (V_{RESET}) for the Pt/ SiO_x /Si device were -2.6 V and -0.9 V, respectively, and those for the Cu/ SiO_x /Si device were $+0.5$ V and -1.3 V, respectively. The operation voltages were significantly lower than previously reported values. For the Pt/ SiO_x /Si devices, the amplitude of V_{SET} was larger than that of V_{RESET} , while for the Cu/ SiO_x /Si devices, V_{SET} was smaller than V_{RESET} . The Cu/ SiO_x /Si device also exhibited multilevel switching behavior. These observations suggest that different switching mechanisms have governed the switching behaviors for devices with different metal electrodes. It is worth pointing out that when the device was biased at 2.6 V, the electric field strength was 26 MV cm^{-1} in 1 nm silicon oxide layer. The

FIG. 2. (a) A typical optical micrograph of the fabricated SiO_x devices with top electrodes diameters ranging from $25 \mu\text{m}$ to $150 \mu\text{m}$; (b) schematic illustration of the device structure and the IV measurement scheme. A typical device consists of a metal top electrode, a SiO_x layer generated in wet chemical process (Piranha cleaning) and a bottom electrode that is the heavily doped silicon wafer. During the IV characterization, a voltage sweep (or pulse) is applied to the top electrode and the bottom electrode is always grounded.

FIG. 3. Typical switching curves from devices with different top electrodes. (a) Devices with Pt top electrodes exhibit unipolar switching behavior. The SET and RESET voltages are -2.6 V and -0.9 V, respectively; (b) Devices with Cu top electrodes exhibit bipolar switching behavior. The device started with OFF state and is forming-free. The SET and RESET voltages are $+0.6$ V and -1.3 V, respectively. The thickness of Pt and Cu electrodes is 12 nm and 24 nm , respectively, and the diameter of all electrode is $50 \mu\text{m}$.

electric field strength was still less than reported hard-breakdown voltage for thin silicon oxide (47 MV cm^{-1}).²⁹

The SiO_x based devices also exhibited repeatable resistive switching behavior with high uniformity. Figure 4(a) shows the first 115 direct current (DC) switching cycles of a $50 \mu\text{m}$ Pt/ SiO_x /Si device. The switching voltage pair (V_{SET} and V_{RESET}) for each switching cycle is plotted in Figure 4(b). Statistical analysis showed that the variation of V_{SET} and V_{RESET} were 5.22% and 11.82% , respectively, demonstrating excellent cycle-to-cycle uniformity for this device (Figure 4(c)).

Electrical characterization and data analysis provides strong evidence that conductive filaments have played a critical role in the device switching behaviors. The filament governed switching can be confirmed by area independent switching behaviors. We measured the IV characterization of Pt/ SiO_x /Si devices with electrode sizes of 50 , 75 , and $100 \mu\text{m}$. For all the devices, the resistance level was at $10^2 \Omega$ range for ON state and $10^5 \Omega$ range for OFF state, with negligible correlation with the device dimension. The independence between the resistance level and electrode size indicates that within the tested length scale, there were only certain number of conductive filaments that have acted as switching centers during the switching.

FIG. 4. Switching uniformity for a Pt/SiO_x/Si device. (a) IV curves for 115 cycles of DC sweeps; (b) the device resistance at different states is independent on lateral dimension due to a filamentary mechanism; (c) the switching voltage in each cycle of DC sweep. The switching voltage is defined as when the current change was more than one order of magnitude after 0.02 V sweep step; (d) cumulative distribution function (CDF) of switching voltages shows that the variation of SET and RESET voltages are, respectively, 5.22% and 11.82%.

The filament composition and formation/rupture process were different for devices with different electrodes. It is well known that the switching behavior for devices could result from different mechanism.⁷ For devices with active metal electrodes such as Cu, the switching is based on cation generation and movement under an electric field, as has been established in electrochemical metallization (ECM) theory

(Figure 5(a)). The theory has also been used to explain previously reported silicon oxide based resistive switching devices.^{30–32} Specifically, the metal (Me) atoms at the top electrode/SiO_x interface were oxidized under the electric field

Under a positive bias on the top electrode, the Me⁺ ions migrated into the SiO_x layer towards the bottom electrons and were reduced into metal atoms

The metal atoms accumulated and formed a conductive filament that bridged the top and bottom electrodes. This metal dissolution and deposition induced by the redox reaction was responsible for the SET process.

The RESET process can also be explained by the redox reactions. When a negative voltage was applied to the top electrode of a device that was at ON state, the metallic bridges were oxidized according to Eq. (1). The oxidation

FIG. 5. Schematic of the switching mechanisms for devices with different top electrodes. (a) SiO_x layer with top electrode of active metal (Cu) is based on cation generation and migration inside of SiO_x. The Cu⁺ ions dissolved at anode interface, travelled to the other side under applied bias, and were reduced to Cu metal, leading to the formation or rupture of a conductive metal filament depending on the polarity of applied voltage; (b) switching of devices with inert metal top electrode (Pt). Conductive filament is formed within SiO_x after SET process.

process took place at the bottom of the metal bridge on the electrode/oxide interface. Under the negative bias on the top electrodes, the resultant metal ions were attracted into the oxide, leading to a rupture in the metallic filament, thus, the RESET process. During both SET and RESET processes, there were discrete intermediate states, and thus exhibits multilevel behavior. It is because multiple filaments formed at ON state, and during SET/RESET process, the filaments were formed/disrupted one by one.

The RESET voltages were usually larger than that for the SET process. This fact can be explained by the nanoscale metal bridge inside of the SiO_x acting as a voltage divider. During the SET process, nearly all the voltages were directly applied on the TE/oxide interface, while in the RESET process, only part of the voltage on the top electrode was actually applied to the BE/oxide interface due to the existence of the voltage divider. Consequently, higher voltages were required so that equivalent amount of the voltages would be delivered to the BE/oxide interface for to dissolve the Ag or Cu atoms into ions for RESET process.

For devices with inert metal, the mechanism is totally different (Figure 5(b)). To further understand the device switching behavior, we fit the IV measurement data according to different models for the ON and OFF states for the 115 switching cycles of the Pt/ SiO_x /Si device. It was discovered that in the ON state, the conduction was governed by an Ohmic model (Fig. 6(a)). The Ohmic behavior for ON state was observed before for a Pt dispersed SiO_x device,³³ and the Ohmic ON state was explained by metal-insulator transition of random material. But it was a bipolar resistive device. Given the switching behavior is independent on voltage polarity, the mechanism is most likely related to thermochemical reaction. The independence of device behavior with the lateral dimension supported a filamentary conduction

mechanism. It is likely that in the SET process, the voltage on the top electrode generated a current and hence Joule heating, which facilitated the formation of the conductive filament. In the RESET process, the filament was ruptured due to thermal breakdown. However, TEM analyses are needed to give us detailed information about the size, location, and composition of the conductive filament(s).

In OFF state, the current-voltage relation was apparently not linear, so the conduction mechanism was different. Chang *et al.*²³ reported a resistive switching device with the oxide layer fabricated by magnetron sputtering in Ar and O_2 ambient, and their OFF state conduction was dominated by Frenkel-Poole (FP) emission. Mehonic *et al.*²⁴ reported a device based on co-sputtered suboxide, the OFF state conduction of which was dominated by trap assisted Fowler-Norheim (FN) tunneling. However, neither of the two conduction mechanisms fit our data. The difference in conduction mechanisms may be resulted from the difference in the oxide layer thickness and the defect densities in the SiO_x layer. Our oxide layer was much thinner, and the chemical composition was closer to stoichiometric than the other two, in which the non-stoichiometric SiO_x probably had provided higher density of defects necessary for either FN tunneling or FP emission.

Data analysis in Figures 6(b)–6(d) show that at low voltage region (0–0.3 V), the current-voltage relation was Ohmic. While at medium voltage region (0.3–2 V), the current was best fit to space charge limited (SCL) transport model. At high voltage region, the current became unstable, and finally jumped at 2.6 V (SET). One possible current transport mechanism is described as the following: as the negative bias was applied on the Pt electrode, the energy band bent upwards at the heavily p-doped Si surface (substrate), which caused high concentration of two-dimensional electron gas (2DEG) accumulated at Pt/ SiO_x interface. The

FIG. 6. Conduction mechanism for a Pt/ SiO_x /Si device. (a) Fitting curve for a device in ON state. In ON state, continuous silicon nanocrystals conduction path was formed which leads to Ohmic conduction; (b) current-voltage curve for a device in OFF state. (c) When the applied voltage is less than 0.3 V, the current follows Ohm's law, (d) while the voltage is between 0.3 V and 2.0 V, the current is dominated by space-charge limited transport (the Mott-Gurney law).

electrons emitted and injected into SiO_x layer under the applied electric field. At low voltage regime, the current was dominated by mobile ion transport, so the current simply followed Ohmic model. At medium voltage regime, the space-charge limited effect occurred because there were limited carriers or traps in the dielectric layer, and the injected carriers controlled electric field profile. According to the Mott-Gurney law,³⁴ the space-charge-limited current was governed by $I = \frac{9}{8} A \epsilon_i \mu / d_i^3 \cdot V^2$, where ϵ_i is dielectric permittivity, μ is the carrier mobility, A is the area, and d_i is the length along the current flow direction. Our data in the medium voltage range fitted the SCL model very well (Figure 6(d)). When the voltage was larger than 2.0 V, part of the current contributed to the formation of silicon nanocrystals, until the device was finally turned to ON state at 2.6 V.

Finally, the low programming voltages for our devices were attributed to the thin silicon oxide layer. Previously, it was reported that for a Cu/SiO_x/Pt device, the forming voltages were proportional to the oxide thickness for devices with 5 nm to 20 nm thick oxide, and the SET voltage is expected to be logarithmically dependent on the thickness ($V_{\text{SET}} = 1.5$ V for a 5 nm oxide device).³¹ While for a SiO_x devices with inert top electrode, the SET voltage stayed at around 4 V for devices with 10 to 200 nm thick oxide,²¹ and the devices required much larger forming voltage.¹⁹ In the current study, the programming voltages were much lower with a 1 nm SiO_x, and both types of the devices were forming-free. The lower operation voltages indicated that the switching behavior may scales with the oxide layer thickness in the sub-5 nm regime.

In summary, we have developed SiO_x based memristive devices that required low programming voltages. The repeatable nonvolatile switching behavior clearly demonstrated that the thin layer of SiO_x produced during Piranha process can be used as the switching material for memristive devices. The simplicity of the device process and the choice of the materials make this device compatible with the current CMOS infrastructure. We also demonstrated that the switching behavior can be explained by either the cation motion model or the formation and annihilation of silicon nanocrystals. The fact that these devices can be switched at low voltages opens venue for the integration of these devices with the state-of-the art ultralow power CMOS circuits.

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