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Spring May, 2013

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Abdelaali Fargi, Faculty of Sciences of Monastir
Neila Hizem
Adel Kalboussi

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Investigation of the kink effect in indium-doped silicon for sub 100 nm N channel MOSFET technology

Abdelaali Fargi*, Neila Hizem and Adel Kalboussi

Laboratoire de Microélectronique et Instrumentation, Departement de Physique, Faculté des Sciences de Monastir, Avenue de l’Environnement, Monastir 5000, Tunisia
Email: fargi.abdelaali@gmail.com
Email: neila_tn2002@yahoo.fr
Email: adel.kalboussi@fsm.rnu.tn
*Corresponding author

Abstract: The increasing interest in nanoelectronic devices that require cryogenic temperatures to function has led to an increased need for analog CMOS circuits. Using indium, an acceptor dopant in silicon, a heavy atom with a low diffusion coefficient is potentially suitable for doping the channel of CMOS transistors. These transistors when operated at low temperatures at which the majority of carriers experience freeze-out exhibit an effect known as the kink effect. In this paper, we will discuss the kink effect presented in the drain current–voltage measurement curves at low temperature. The variation of conductance and transconductance was calculated from measurements of the drain current versus gate and drain voltages. Capacitance-voltage versus temperature was measured to investigate the freeze-out of carriers that could be related to indium in the p-type doping region and then Deep Level Transient Spectroscopy (DLTS) measurement was carried out to determine the trap level and its activation energy. The effect of traps related to indium in Si NMOS transistors is investigated with the DLTS technique and the existence of a relationship between the kink effect and the active indium trap level situated at 0.18 eV from valence band is also discussed.

Keywords: Si MOSFET; I–V characteristics; DLTS; impact ionisation; kink effect; retrograde doping profile; indium trap level; nanotechnology.


Biographical notes: Abdelaali Fargi received the Master of Science Degree in Materials Science and Nanostructures from Faculty of Sciences of Monastir, Tunisia, in 2010. He is currently working towards a PhD degree at the Department of Physics, Monastir University, Tunisia. His PhD research topic is parasitic effects on the characteristics of the indium-doped silicon MOSFETs.

Neila Hizem is an Associate Professor of Physics at the Department of Physics in Faculty of Sciences of Monastir. She received the Bachelor of Science in Physics from Faculty of Sciences of Monastir, Master of Science in Materials Science for integrated electronics from INSA Lyon and the PhD degree in the same field from INSA Lyon.
1 Introduction

The short-channel effect in MOSFETs is one of the major problems in miniaturisation and to remedy this problem, several authors have [1–5] studied the case of a non-uniform doping substrate. The non-uniform doping of the substrate, in particular retrograde doping, limits the flow of electrons from source to drain at zero bias of the gate. The retrograde doping reduces the extension of the space-charge zone and thus reduces the interaction between the source and drain. For its low diffusion coefficient and its higher solubility limit compared with other dopants in silicon like boron, aluminium and gallium, we focus our study on indium-doped silicon for its important use in scaling devices. Even with the advantages of indium-doped silicon, when scaling down dimensions of MOSFETs, many parasitic effects appear like the kink effect. This parasitic effect, which is characterised by a sharp increase in the drain-source current at a certain drain-to-source voltage \( V_{ds} = V_{kink} \), yields a high drain conductance. Many studies of the kink effect in field effect transistors such as MOSFETs (bulk and SOI) and HEMTs have been reported, but due to its complex behaviour, the origin of this effect is still a subject of interest. Some studies have established a link between the kink effect and the impact ionisation phenomenon occurring in the channel [6], while other studies have correlated this effect with the presence of traps in the structure [7]. Other studies [8] have reported the impact ionisation depends on a hole trapping and detrapping phenomenon in HEMTs.

The aim of this work is to discuss the relative influence of the kink effect compared with the activation of indium in silicon. To that end, a detailed study of the electrical characteristics of deep levels was performed using transient spectroscopy (DLTS) technique. In order to study the impact of deep trap levels on the kink effect, drain current measurements were carried in 86–295 K temperature range. The drain current is measured to determine the maximum of conductance and transconductance in the kink region and then make a link between these maximums and the trap level deduced from DLTS results.

2 Experiments

N’P well diodes and NMOSFET transistors were fabricated to study the effect of dopant redistribution. These devices were investigated in each case using a retrograde well indium and boron implantation as shown in Figure 1, which was deduced from capacitance-voltage profiling. A P well of about \( 5 \times 10^{17} \text{ cm}^{-3} \) indium implanted was formed in a P substrate at 100 nm under the interface. Boron implantation was performed to adjust the substrate doping to about \( 10^{17} \text{ cm}^{-3} \). The NMOSFET device had a gate oxide
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thickness of 3.2 nm. The surface of the active zone of the poly gate NMOSFETs was 100 × 100 µm² (LxW). N⁺P well diodes fabricated with 5 × 10¹⁶ cm⁻³ for both In and B dopants were used for testing the MOS devices. A variety of methods, DLTS and I-V-T, have been used to characterise the acceptor levels related to the presence of indium in N⁺P well diodes and MOS transistors.

Figure 1 Retrograded doping profile showing indium and boron concentration deduced from capacitance-voltage profiling

2.1 I–V characteristics versus temperature

The electrical characterisation of N channel MOSFET transistors for different temperatures gives us the main results as shown in Figure 2.

Figure 2 ID–VD characteristics of an NMOSFET showing the kink effect for different gate voltages and temperatures: (a) T = 86 K, (b) T = 124 K, (c) T = 173 K, (d) T = 230 K (see online version for colours)
Figure 2  ID–VD characteristics of an NMOSFET showing the kink effect for different gate voltages and temperatures: (a) $T = 86\, \text{K}$, (b) $T = 124\, \text{K}$, (c) $T = 173\, \text{K}$ and (d) $T = 230\, \text{K}$ (continued) (see online version for colours)
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Figure 2 ID–VD characteristics of an NMOSFET showing the kink effect for different gate voltages and temperatures: (a) \( T = 86 \) K, (b) \( T = 124 \) K, (c) \( T = 173 \) K and (d) \( T = 230 \) K (continued) (see online version for colours)

![Figure 2](image)

Figure 2a–2d shows the static output characteristics (\( I_{ds}–V_{ds} \)) of the transistor at 86, 124, 173 and 230 K, respectively. We notice that the drain current continues to increase even in the saturation region. This unusual variation of the drain current is well known as the kink effect [10]. It consists of a sharp increase in the drain-source current at a certain drain-to-source voltage \( (V_{ds} = V_{kink}) \). This variation of the drain current induces an increase of the drain/source output conductance \( (g_{ds}) \) and a decrease of the amplification factor. Kink effect appears at low temperatures \( (T \leq 300 \) K) with a clear increase in drain current. We observe that when the gate voltage increases, the amount of drain current and kink voltage increases too. As temperature decreases, we note that the excess of drain current increases, especially at \( T = 124 \) K.

2.2 Deep level transient spectroscopy measurements

Owing to their low gate capacitance, DLTS measurements cannot be performed on MOSFETs. To overcome this problem, DLTS measurement has been carried out on \( N^+P \) junctions that were fabricated using the same substrate and conditions. In order to investigate the freeze-out of carriers and the presence of the hole traps \( C(V, T) \) and DLTS were performed. Figure 3 shows the capacitance-voltage at different temperatures and at frequency 100 kHz. At zero bias, the capacitance value arises from 92 pF at 100 K to 143 pF at 300 K. The difference between the \( C–V \) curves is small when the reverse voltage exceeds 2 V. DLTS measurements, as shown in Figure 4, were performed in 40–300 K temperature range using the lock-in amplifier technique (A–B) for different emission rates. The \( N^+P \) junction is negatively biased to obtain a depletion zone and it is pulsed to the equilibrium state to show the emission of traps.
From Figure 4, we have calculated the signature of the indium trap level that gives activation energy of 0.18 eV, capture cross-section of $7 \times 10^{-13}$ cm$^2$ and trap density of $3 \times 10^{15}$ cm$^{-3}$. The indium level investigated in our study is in good agreement with the literature [9] and it presents a strong field effect such that its activation energy varies from 0.15 eV to 0.2 eV.
3 Analysis of the kink effect

To analyse the kink effect, we plot the change in drain current in the kink zone according to the kink voltage (Figure 5), and the gate voltage $V_G$ for different temperatures.

The slopes of the $\Delta I_{\text{kink}}-V_G$ and $\Delta I_{\text{kink}}-V_{D\text{kink}}$ curves for different temperatures were calculated which are illustrated in Table 1.

In Table 1, we observe a maximum of both channel conductance and transconductance at a temperature of 124 K, where the indium trap level seems to be responsible of these maximums.

Figure 5  The plot of $\Delta I_{\text{kink}}$ measured from output characteristics versus $V_G$ (a) and versus $V_{D\text{kink}}$ (b) (see online version for colours)
As well-known from the literature [10–11], the appearance of excess drain current in the saturation region of MOSFET/SOI (the so-called kink effect) arises from the threshold voltage shift due to the forward biasing of the source-substrate diode caused by substrate impact ionisation current flowing from the drain to the source. In practice, a similar situation occurs in bulk silicon MOSFETs operating at very low temperature [12] or when disconnecting the substrate electrode at room temperature [13]. The impact ionisation is directly related to the avalanche phenomenon. Indeed by increasing the voltage $V_{DS}$ beyond the pinch-off voltage, the drain field becomes strong enough to ionise atoms in channel area of space-charge in drain side. These highly energetic electrons are able to extract other electron–hole pairs. The created electrons contribute strongly to the conduction channel. The holes are attracted towards the gate, but others are attracted towards the substrate thus causing a gate–substrate current resulting in an increase of the drain current too [14–16]. This ionisation can also attack the traps in the substrate where a generation and recombination will induce an additional current. However, for temperatures below the room temperature the connection of the substrate is insufficient to cancel the kink effect.

In addition to impact ionisation, some works show the correlation between trap level and the kink effect [7, 17–18]. By measuring the surface of hysteresis versus temperature in the literature [7, 17], it was found that the maximum of hysteresis area appears at the temperature where the trap level was detected by current DLTS.

In our case, we have measured the excess of drain current versus gate and drain voltages and we have obtained the maximum of both transconductance and conductance at a temperature range where the trap level was detected by DLTS.

We understand that the problem arises when decreasing the gate length. Indeed, this decrease was such that the channel zone is not quite rectangular, and one cannot overlook the influence of the drain channel interface beneath the gate. Traps in the space-charge region in the drain lateral side will be influenced by both the gate along the x-axis direction (perpendicular to the channel) and the drain along the two axes x and y (perpendicular and parallel to it). Part of the voltage $V_{DS}$ will then be superimposed negatively to the gate. By applying a positive $V_{GS}$ the hole trap will capture the electrons since the Fermi level rises. By applying a low voltage $V_{DS}$, all the voltage appears along the y-axis direction to drain the electrons from the source to drain. Gradually, as the voltage $V_{DS}$ increases, the component along the x-axis direction $V_{DS}$ also increases until a critical voltage (called $V_{kink}$) sufficiently lowers the Fermi level again and causes the trap to eject the trapped electrons in the pinched area. The channel is reconstituted and becomes conducting. The current is linear with almost the same slope and saturates again.

This leads us to believe that both the substrate effect and trapping/detrapping by a deep level centre are responsible of the increase of drain current.
4 Conclusion

In summary, deep levels in a PN junction were directly measured by means of the DLTS technique. I–V measurements were also performed on N channel MOSFET transistors. The I–V characteristics versus temperatures have shown the presence of the kink effect in the structure. The analysis of the excess drain current versus drain and gate voltage shows the maximums of both conductance \( g_d \) and transconductance \( g_m \) at around \( T = 124 \, \text{K} \) when the indium level is activated. This leads to the hypothesis that there is a correlation between deep level of indium situated at 0.18 eV and the observed kink effect in all I–V characteristics.

References


